6322

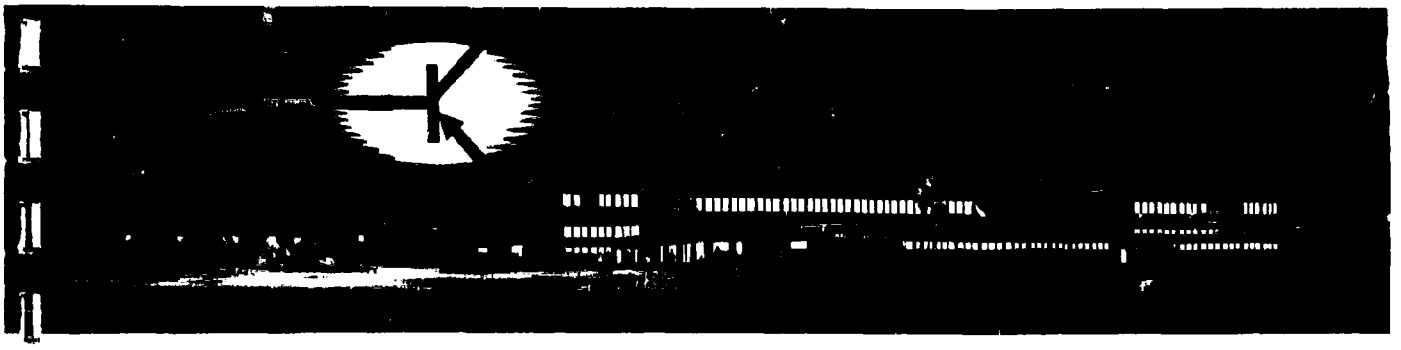
FIFTH QUARTERLY REPORT
COMPATIBLE TECHNIQUES
FOR
INTEGRATED CIRCUITRY

U. S. AIR FORCE
CONTRACT NO. AF33(616)8276

Period Covered
1 May 1962 to 31 July 1962

prepared for

U. S. AIR FORCE
AERONAUTICAL SYSTEMS DIVISION
WRIGHT-PATTERSON AIR FORCE BASE, OHIO



MOTOROLA Semiconductor Products Inc.
5005 EAST McDOWELL ROAD PHOENIX, ARIZONA A SUBSIDIARY OF MOTOROLA INC

FIFTH QUARTERLY REPORT

COMPATIBLE TECHNIQUES FOR INTEGRATED CIRCUITRY

PERIOD OF

1 MAY 1962 to 31 JULY 1962

UNITED STATES AIR FORCE

CONTRACT NO. AF 33(616)-8276

Prepared for . . . . . .

UNITED STATES AIR FORCE

AERONAUTICAL SYSTEMS DIVISION

WRIGHT-PATTERSON AIR FORCE BASE, OHIO

Prepared by . . . . . .

MOTOROLA, INC.

SEMICONDUCTOR PRODUCTS DIVISION

PHOENIX, ARIZONA

INDEX

1.0 INTRODUCTION

This report covers the fifth quarter's efforts in developing Compatible Techniques for Integrated Circuitry on contract AF 33(616)-8276.

Most of the effort to date has been spent in developing process techniques which are necessary for Integrated Circuit fabrication. This effort has been both in morphological areas and thin films as applied to semiconducting substrate.

Further efforts in perfecting our epitaxial techniques are reported. A program has been started to develop and fabricate typical circuits which are practical for a wide range of high and low frequency amplifier applications as well as logic circuits.

2.0 BASIC MATERIAL STUDIES

2.1 Open Tube Epitaxial GaAs

The gas flow system was redesigned to obtain better control. The present system is shown in Figure 1.

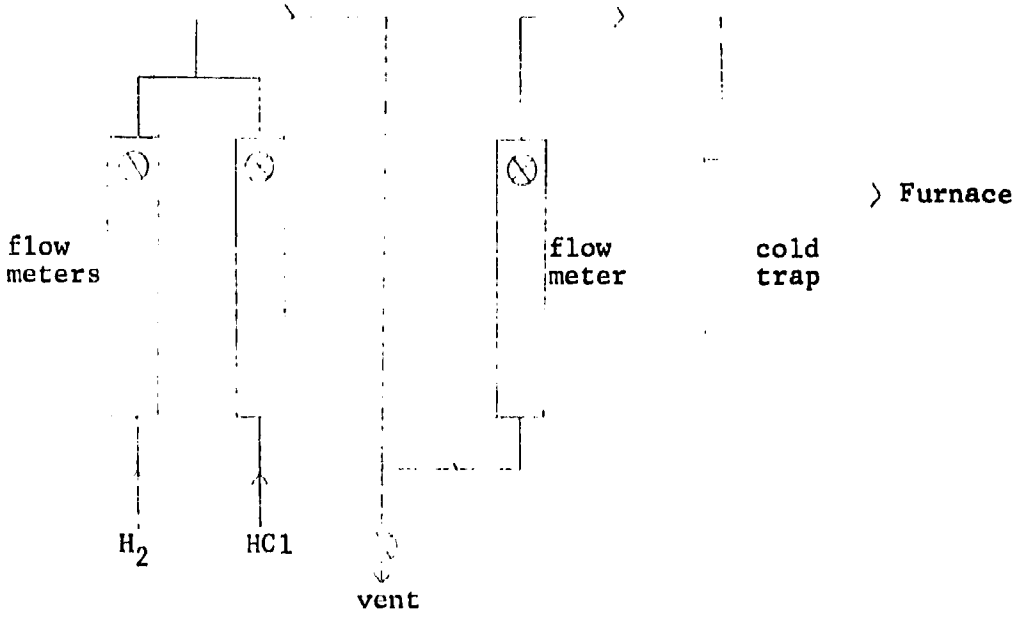


FIGURE 1

Several intermittent leaks were detected and closed. The HCl supply was replaced and the H_2 purity checked to eliminate as much contamination as possible. Oxygen content of the H_2 after purification reads 1.3 ppm.

The quartz boats are being etched in the furnace between runs. Hydrogen and HCl are mixed and added as an etchant over the deposition area of the boat which is held at about 1050°C.

P-type (111) wafers are being used as substrates. This will allow capacitance measurements of the film to be made and allow easier thickness determinations.

N-type films have been deposited on P-type GaAs substrates for evaluation purposes. The interface appears flat and without apparent diffusion. The etchant used for developing the interface consists of 10 ml of 5% naOH and one drop of H_2O_2. See Figure 2. Mesas were etched on several samples and breakdowns measured at 8 - 10 volts without attempts at controlling surface conditions. Carrier concentration of the P-type substrate was approximately $10^{17}/cm^3$. Capacitance measurements made on these films indicate the film carrier concentration to be somewhat higher than $10^{17}/cm^3$. More definite data can be obtained on higher doped substrates.

Deposition has been occurring during the preheat cycle without the presence of a minimum amount of HCl. The gas system was further modified to insure no release of hung-up HCl during the hydrogen purge and preheat. Analysis of the gas stream through $AgNO_3$ indicates no HCl present. The possibility remains that a small amount of oxygen in the gas stream could be transporting gallium and leading to deposition of GaAs on the substrates. This deposition is epitaxial and although quite thin, is uncontrolled. If the transporting agent cannot be found and eliminated, deposition on the wafers can be reduced by changes in the gas flows during the preheat.

FIGURE 2
Epitaxial N on P Beveled and Stained
Film Thickness is 2.4μ

Deposition occurring during the preheat cycle under a H_2 atmosphere was studied during this period. As previously reported, the film is epitaxial, but uncontrolled. Current tests indicate a one-hour preheat is necessary to bring boat, source and substrates to temperature before introducing growth flow rates.

Although a palladium silver alloy diffusion unit was used as the source of pure hydrogen, hygrometer readings indicate some moisture present. A small amount could possibly be transporting gallium and causing pre-deposition on the substrates. Extensive measures have been taken to reduce the moisture content by utilizing molecular sieve drying towers and dry ice and acetone cold traps, but the problem remains. The dry ice and acetone traps proved unsatisfactory since any moisture trapped reacted with the hydrogen chloride gas forming hydrochloric acid. A certain amount of hydrogen chloride gas passed through the cold trap and the growth reaction was carried out. Since the growth rate is very dependent on the percentage of HCl in the gas stream, small variations in the HCl content caused by the reaction in the cold trap made control of the growth rate difficult.

To side-step this problem, a gas phase etching process proved effective. During the preheat cycle an excess of HCl is introduced and the H_2 increased from 300 cc/min. to 1000 cc/min., therefore, decreasing the efficiency of the HCl over the source. The HCl does not reach equilibrium over the source and continues to etch the substrates. At a mixture ratio of 800:1 (H_2:HCl) with a total flow stream of 1000 cc/min.; smooth, planar etched surfaces were obtained on the GaAs <111> B face.

Growth conditions are established subsequent to the etch cycle by decreasing the total concentration of H_2 + HCl to 300 cc/min. at a ratio of 1000:1 (H_2:HCl). Film surfaces appear as an inverted "orange peel" effect. This can be rectified by varying flow rates and amount of source.

Initial experiments have not produced comparable results on the GaAs <111> A face. A one-zone resistive furnace and apparatus is being assembled for further development of gas phase etching.

2.2 Incremental Sheet Resistivity in Doped P-type Films

2.2.1 Material

Two epitaxial wafers, 1012-9 and 1012-7 were used in these anodizations. The N-type substrate of both had a bulk resistivity of 0.01 Ω cm to 0.02 Ω cm. The P-type epi-film of 1012-9 has a bulk resistivity of 0.096 Ω cm and an estimated (from the growth curve) depth of 3 μ. The N-type substrate was arsenic doped and gas etched before the boron doped epi-film was grown automatically.

2.2.2 Procedure

A piece from the edge of 1012-9 was removed, beveled and stained to check the P-layer thickness. The depth varied from 1.77 μ to 2.07 μ for an average of 2.01 μ. A mesa area of 0.635 cm^2 was etched on each wafer by immersion in CP-4 for 30 seconds.

The anodization apparatus was set up[1] and 10 minute runs were carried out on each wafer. After each run, the oxide was removed with HF. After every third run, the sheet resistivities were measured and after every ninth run, the wafers were weighed. Both wafers probed N-type after 39 runs. The amount of silicon removed was calculated for each wafer using the weight loss, density of silicon and mesa area. The average resistivities, $\bar{\rho}_L$ (ohm-cm), in the removed layers, Δt(cm), were calculated using the formula:

$$\bar{\rho}_L = \left| \frac{4.4E_2E_1}{I_2E_1 - E_2I_1} \right| \Delta t$$

were E_2 is the voltage drop (volts) across the four-point probe points before removal of Δt; E_1 is the voltage drop across the points after removal of Δt; I_2 is the current flow after removal of Δt.

2.2.3 Results

The results of the two experiments are summarized in Table 1.

The total amount of silicon removed from each wafer was 3.64 μ, slightly more than that originally predicted, 3 μ. The average amount determined by staining a piece of 1012-9, 2.01 μ, was much less that the amount removed. This large discrepancy may be due to a falling off in epitaxial growth near the edges of the

[1] J. E. McNamara and H. M. Robertson, "METHODS FOR MEASURING RESISTIVITY GRADIENTS AND THICKNESSES IN EPITAXIAL FILMS," Technical Note #9, Material Diffusion Laboratory.

TABLE I

	1012-9		1012-7	
Run	Δt By Weight	$\bar{\rho}_L$	Δt By Weight	$\bar{\rho}_L$
3	0.28 μ	0.2546 Ωcm	0.28 μ	0.1867 Ωcm
6	0.28	0.1167	0.28	0.0933
9	0.28	0.1000	0.28	0.0824
12	0.28	0.1037	0.28	0.0933
15	0.28	0.1273	0.28	0.1000
18	0.28	0.1037	0.28	0.0903
21	0.28	0.1037	0.28	0.0903
24	0.28	0.1037	0.28	0.0903
27	0.28	0.1167	0.28	0.1037
30	0.28	-	0.28	0.1000
33	0.28	-	0.28	0.1167
36	0.28	-	0.28	-
39	0.28	-	0.28	-

wafer. Previous to these anodizations, a piece near the edge of wafer 1012-8 was beveled and stained and found to have a P-layer depth of 3.52 μ average.

A comparison of the resistivities obtained by using Δt from the color method (published values for oxide thickness as a function of interference color) and Δt derived from the staining method are summarized in Table 2.

TABLE 2

	1012-9				1012-7			
Run	Δt By Color	$\bar{\rho}_L$ By Color	Δt By Stain	$\bar{\rho}_L$ By Stain	Δt By Color	$\bar{\rho}_L$ By Color	Δt By Stain	$\bar{\rho}_L$ By Stain
3	0.33μ	0.3000 Ωcm	0.16μ	0.1455 Ωcm	0.33μ	0.2200 Ωcm	0.16μ	0.1067 Ωcm
6	0.33	0.1375	0.16	0.0667	0.33	0.1100	0.16	0.0533
9	0.33	0.1178	0.16	0.0571	0.33	0.0971	0.16	0.0471
12	0.33	0.1222	0.16	0.0593	0.33	0.1100	0.16	0.0533
15	0.33	0.1500	0.16	0.0727	0.33	0.1178	0.16	0.0571
18	0.33	0.1222	0.16	0.0593	0.33	0.1065	0.16	0.0516
21	0.33	0.1222	0.16	0.0593	0.33	0.1065	0.16	0.0516
24	0.33	0.1222	0.16	0.0593	0.33	0.1065	0.16	0.0516
27	0.33	0.1375	0.16	0.0667	0.33	0.1222	0.16	0.0593
30	0.33	-	0.16	-	0.33	0.1178	0.16	0.0571
33	0.33	-	0.16	-	0.33	0.1375	0.16	0.0667
36	0.33	-	0.16	-	0.33	-	0.16	-
39	0.33	-	0.16	-	0.33	-	0.16	-

2.2.4 Discussion

Sheet resistivity readings were taken with a 25-mil germanium probe. The points on this probe are rounded in comparison to the points of 25-mil and 50-mil silicon probes used in previous experiments. It appears that the rounded points permit readings to be taken after a larger number of anodizations than the sharper points. The surfaces measured with the sharp points are scratched and marred suggesting that the points penetrate through the P-layer.

Bulk resistivities calculated from sheet resistivity readings taken before anodization and the total depth are higher than those reported in both cases, 0.1184 vs. 0.096 Ωcm for 1012-9 and 0.1027 vs. 0.084 Ωcm for 1012-7. The resistivities after the first three anodizations show a sharp decrease. The resistivities drop and then reach another peak about one-third of the distance through the layer before leveling off. As the junction is approached, the curve slopes upward. The similarity between the two curves is striking. Even the points lying off the curves are approximately the same distance away from their respective curves.

Both the color and the staining methods prevent problems which cannot be ignored. It was observed previously[2] that the weight change method indicates a 20% less thick silicon removal than would be calculated from published values for oxide thickness as a function of interference color. These experiments show a 15% less thick silicon removal. The staining method is probably not accurate when measurements are taken as close to the edge of the wafer as they are in this case.

---

(2) Op. Cit.

2.3 Sheet Resistivity Gradients Through Epitaxial Films

2.3.1 Material

Six silicon wafers were anodized since the last report and resistivities were measured after every third anodization. Wafer 525-2 ($P\text{-}n\text{-}N^+$ structure; P-layer 0.0587 Ωcm; N^+ -substrate 0.0032-0.0015 Ωcm) was anodized 28 times before the N-layer was reached. Wafers 505-1 ($P\text{-}N\text{-}N^+$ structure; P-layer 0.0372 Ωcm; N^+ -substrate 0.015-0.025 Ωcm) and 505-2 ($P\text{-}N\text{-}N^+$ structure; P-layer 0.0585 Ωcm; N^+ - substrate 0.015-025 Ωcm) were anodized 28 and 10 times respectively. Wafers Z-14-6, Z-14-7 and Z-14-8 (P-N structure; P-layer 0.00745 Ωcm; N-substrate 0.1 Ωcm) were anodized 15, 44 and 23 times respectively.

2.3.2 Procedure

Various oxide thicknesses were grown on each wafer by increasing the current density and/or increasing the anodization time in order to speed up the entire process. Wafers Z-14-6, 7 and 8 were also anodized with the apparatus[3] slightly modified so that two wafers could be anodized at the same time. The modifications consisted of two holes being cut into the polyethylene beaker and two rubber seals being used. A t-shaped piece of glass tubing was inserted into the surgical tubing and two polyethylene tubes were attached to this by more surgical tubing. Thus, the circulating pump sent the electrolyte through the T-tube and onto

(3) J. E. McNamara and H. M. Robertson, "METHODS FOR MEASURING RESISTIVITY GRADIENTS AND THICKNESSES IN EPITAXIAL FILMS," Technical Note #9, Materials Diffusion Laboratory

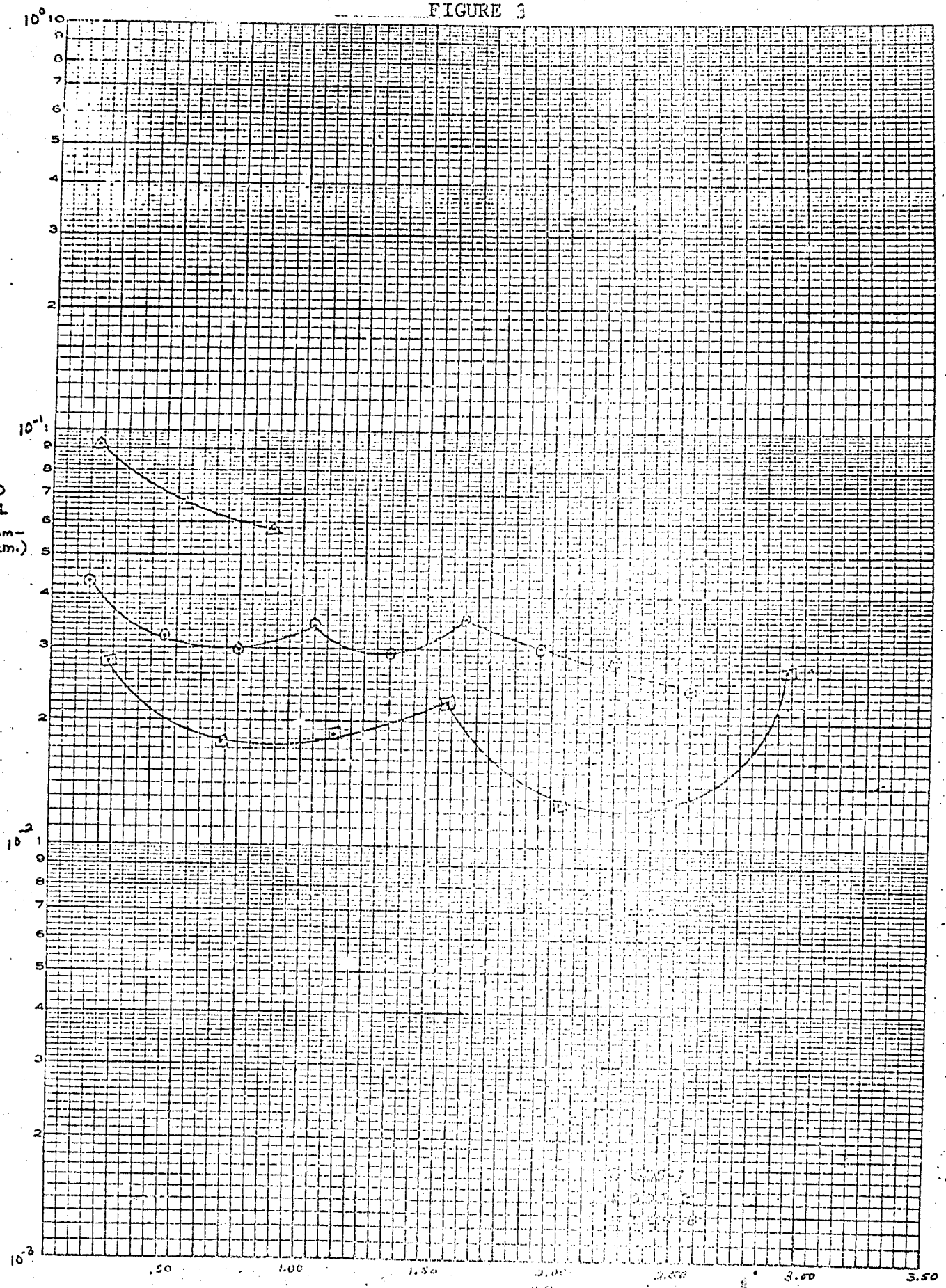
the surface of two wafers at the same time. These modifications decreased the time element by a small amount and allowed the resistivities to be compared as the experiment progressed.

2.3.3 Results and Discussion

Sheet resistivity measurements all showed a dip in the curve for the first 9 to 12 anodizations as shown in Figures 3 and 4, and Table 3. The resistivities appear to be high near the surface of the wafer, decrease after a few increments have been removed, and rise again after a few more are removed. This same curve was also shown for wafers 1012-7 and 1012-9 in the report for May 1962.

There is a striking similarity between the curves of wafers Z-14-6 and 7 which are from the same furnace run. Work will be continued on wafers from a single furnace run to see if they show curves similar to each other.

FIGURE 3



Depth (m) - 13 -

FIGURE 4

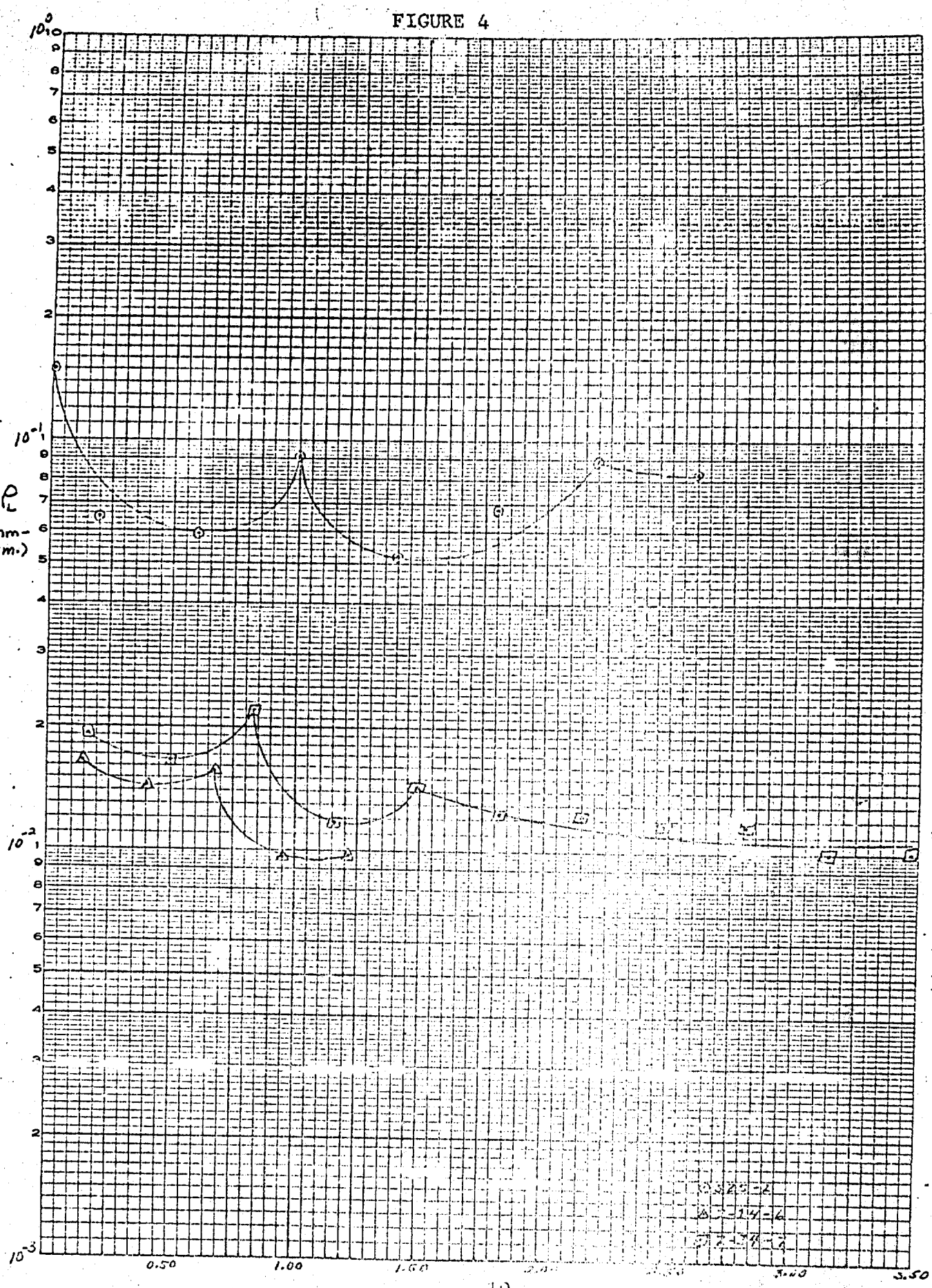


TABLE 3

	525-2		505-1		505-2		Z-14-6		Z-14-7		Z-14-8	
RUN	Δt By Weight	ρ_L Ω cm.	Δt By Weight	ρ_L Ω cm.	Δt By Weight	ρ_L Ω cm.	Δt By Weight	ρ_L Ω cm.	Δt By Weight	ρ_L Ω cm.	Δt By Weight	ρ_L Ω cm.
3	0.06 μ	0.1500	0.30 μ	0.0429	0.35 μ	0.0921	0.27 μ	0.0165	0.33 μ	0.0191	0.45 μ	0.0279
6	0.40 μ	0.0645	0.30 μ	0.0319	0.35 μ	0.0661	0.27 μ	0.0143	0.33 μ	0.0166	0.45 μ	0.0176
9	0.40 μ	0.0588	0.30 μ	0.0297	0.35 μ	0.0574	0.27 μ	0.0156	0.33 μ	0.0220	0.45 μ	0.0185
12	0.40 μ	0.0909	0.30 μ	0.0341	-	-	0.27 μ	0.0096	0.33 μ	0.0118	0.45 μ	0.0223
15	0.40 μ	0.0520	0.30 μ	0.0294	-	-	0.27 μ	0.0097	0.33 μ	0.0143	0.45 μ	0.0126
18	0.40 μ	0.0670	0.30 μ	0.0353	-	-	-	-	0.33 μ	0.0124	0.45 μ	0.0128
21	0.40 μ	0.0889	0.30 μ	0.0303	-	-	-	-	0.33 μ	0.0124	0.45 μ	0.0266
24	0.40 μ	0.0833	0.30 μ	0.0283	-	-	-	-	0.33 μ	0.0117	-	-
27	-	-	0.30 μ	0.0240	-	-	-	-	0.33 μ	0.0117	-	-
30	-	-	-	-	-	-	-	-	0.33 μ	0.0100	-	-
33	-	-	-	-	-	-	-	-	0.33 μ	0.0103	-	-

3.0 THIN FILM TECHNOLOGY

3.1 Vapor Deposition of Glass Films

The purpose of this task is to develop means for depositing glass films onto semiconductor substrates, utilizing the technologies which are compatible with semiconducting materials and with other thin films. The films are under investigation for use as: (a) dielectric films for capacitors, and (b) electrical insulating films for conductor crossover insulation.

A series of investigations were conducted to determine the optimum parameters for deposition of various types of films during this reporting period. Significant results from these investigations include the following: Preliminary results indicate that Al_2O_3 SiO_2 capacitors can be manufactured to tolerances of $\pm 10\%$ in capacitance value.

During this reporting period a group of 15 Al_2O_3 SiO_2 capacitors were fabricated for environmental test purposes. After approximately 400 hours at 125°C with 12 volts DC electrical stress applied, one unit out of fifteen showed electrical short circuiting. Two other units, however, showed evidence of having shorted during the test, with subsequent healing of the shorts by the "burning off" of the top electrode over the shorted area. These healed shorts are reflected by a large decrease in capacitance (30 to 50%) for these units. The remaining capacitors showed an average decrease of about 6% in capacitance. No significant change in leakage current or dissipation factor was noted for the remaining 12 capacitors.

During the previous reporting period, a number of $Al_2O_3 \cdot SiO_2$ capacitors were fabricated at a range of different dielectric deposition temperatures to study the effect on capacitor properties of the temperature of deposition of the dielectric. Evaluation of these capacitors has shown that the dielectric constant of the films is essentially independent of the deposition temperature, the dissipation factor of the films decreases by a small amount as the deposition temperature rises, and the DC leakage current of the capacitors is a comparatively strong function of deposition temperature.

These capacitors will later be put on environmental tests to determine any relationships that may exist between the capacitor life expectation and the dielectric deposition temperature. Figure 1 shows the behavior of capacitance vs. temperature for a capacitor. The temperature coefficient of the capacitor varies from 135 ppm measured at 100 kilocycles per second to 420 ppm when measured at 100 cycles per second.

Life tests on the aluminosilicate capacitors initiated during the previous reporting period were continued this period until a malfunction of the test chamber caused the tests to be terminated after 720 hours of test time. These capacitors were fabricated on five substrates, each substrate containing three capacitors. All six of the capacitors on two of the five substrates failed within the first 50 hours of the test. No failures were detected, however, on the remaining nine capacitors on the other three substrates during the entire test period. It is interesting to note that, discounting the six early failures, that the remaining capacitors accumulated over 6500 unit hours of testing at 12 volts DC potential in an environment of 125°C with no failures.

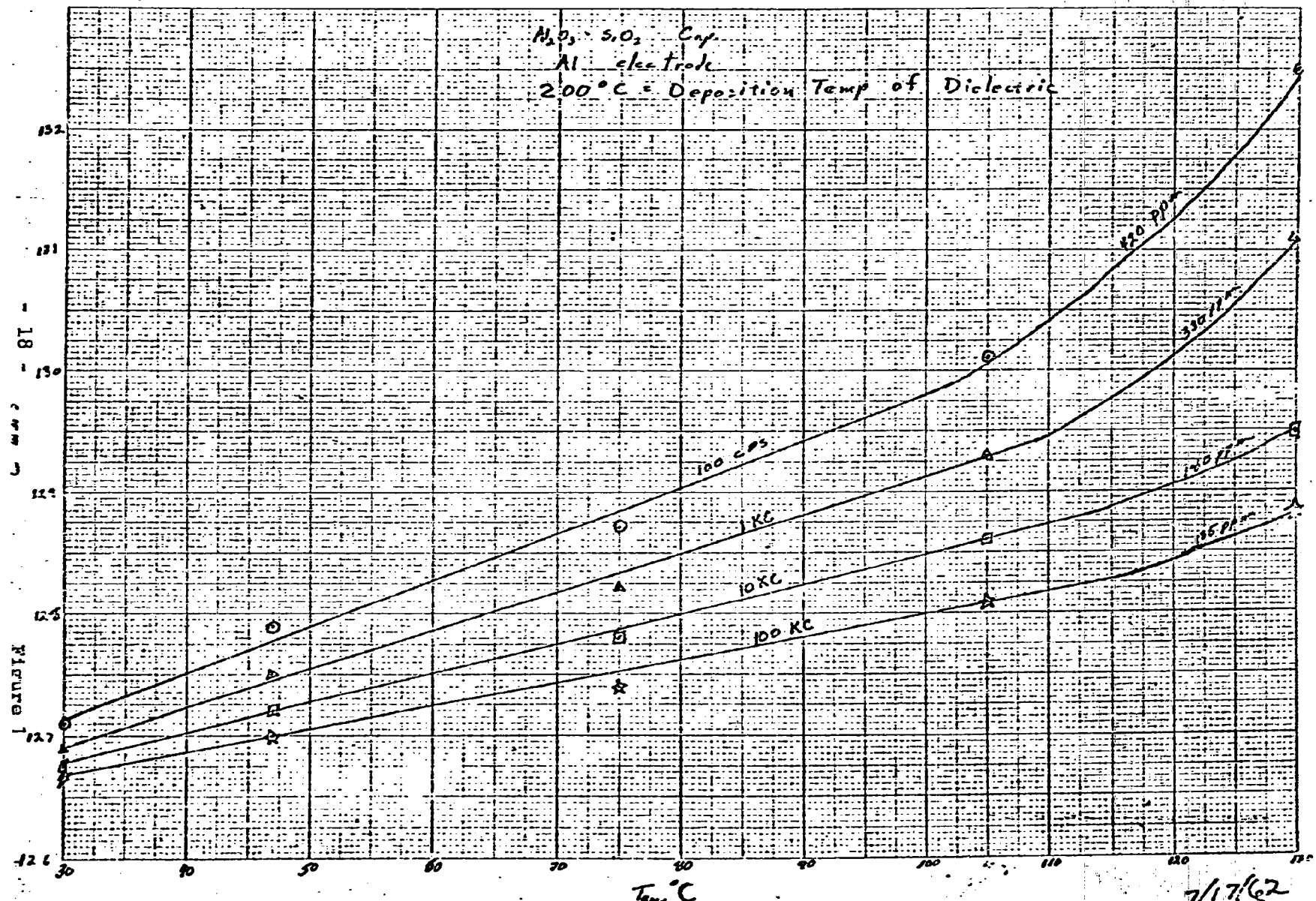


Figure 1

7/17/62

The nine capacitors surviving the life tests exhibited an average decrease in capacitance of 3% over the period of testing. No significant change in dissipation factor or DC leakage resistance was detected.

During the next reporting period a study will be made of the effects of the ratio of aluminum oxide to silicon dioxide in the aluminosilicate capacitors on the capacitor properties. An additional number of capacitors will also be fabricated for further environmental testing.

3.2 Tantalum Oxide Capacitors

Although the new tantalum evaporator is not operating satisfactorily as yet, a small amount of effort was spent on this

phase of the project during this reporting period. Present effort is concerned with the development of a satisfactory method of making electrical contact with the tantalum film for purposes of anodizing. Present methods of establishing such contact involve the use of a seal around the contact area to prevent the anodizing electrolyte from establishing electrical contact with the connection wire. These seals occupy considerable amount of space on a substrate, and do not produce as reliable a seal as is desirable. Methods presently being investigated involve the bonding of a tantalum or aluminum wire to the thin film by ultrasonic and thermocompression techniques.

3.3 Thin Film Inductors for Transceivers

The objectives for this reporting period were to continue the fabrication of 0.08, 0.165, 0.22, 0.47 and 1.0 microhenry inductors on 0.200 inch circular ceramic alumina disks for use in the 120 mc transceiver. Masks for all the values have been received and six samples of the 1.0 microhenry inductor, plus four samples of each of the remaining values have been partially fabricated. Close examination of the available substrates led to a decision not to use the standard glaze. Contrary to the conclusions drawn previously and as outlined in previous reports for this program, it was decided to use the ceramic wafers without glazing.

After the coils were fabricated, it was necessary to build up the thickness and line width of the conductor by electrodeposition of additional copper due to undercutting and etching. The additional plating reduces the electrical resistance, thus increasing the Q value. The plating process is currently being

carried out on four samples of each of the 0.08, 0.165, and 0.22 values, and six each of the 0.47 and 1.0 values.

As mentioned in the previous report, it is more advantageous for the assembly of the coils by thermocompression bonding if the surface of the finished copper conductor is gold plated. Four samples of the 0.22 microhenry coil were prepared in this fashion and submitted for evaluation. These samples then underwent a thermocompression bonding process to attach electrical leads to the substrates, and during this process all the coils lifted from the substrate surface. This problem is currently under study.

During this reporting period, the required number of coils for the transceiver were completed. A thermocompression bond test was made to the spiral inductors which proved to be successful.

Resistance values in ohms for the coils measured after etching (R_1), after additional copper electroplating (R_2), and after gold plating (R_3) are listed for each sample.

Sample	R_1	R_2	R_3
4 Turn 0.08 μh			
1	1.03	.60	.64
2	5.9	.67	.66
3	1.04	.62	.64
4	.94	.63	.65
6 Turn 0.165 μh			
1	2.45	1.08	.99
2	3.70	.91	.92
3	1.96	.99	.99
4	6.10	1.00	1.03

7 Turn 0.22 μh

1	2.05	1.00	.98
2	3.60	1.02	1.02
3	2.80	.98	.99
4	2.80	.90	.91

14 Turn 0.47 μh

1	8.60	2.23	2.27
2	9.50	1.90	1.87
3	5.40	2.08	1.76
4	3.45	1.80	1.84
5	2.90	1.76	1.77
6	5.30	1.90	1.86

19 Turn 1.0 μh

1	5.60	2.85	2.01
3	4.30	2.04	1.96
4	5.30	2.03	1.98
5	4.80	2.30	2.25
6	4.00	2.20	2.10

(#2 lifted from substrate after etch)

A summary of the six principle steps in fabricating these coils follows. The substrates were given a light polish and cleaned by ultrasonic agitation in acetone.

1. Vacuum deposit chrome-copper films.
2. Successively electroplate and polish until a smooth surface is obtained.
3. Photoresist, expose, develop and etch.
4. Clean off photoresist and attach substrate and film with silver paint to approximately one square inch evaporated copper film on glass slides. This slide area serves to reduce current density over the coil surface for smoother plating.
5. Electroplate until desired resistance value is obtained.
6. Clean off excessive copper deposit and silver paste, and gold plate surface by immersion technique. Record final resistance value.

Until further samples are requested, no additional effort will be spent on this phase of the project.

3.4 Silicon Monoxide Capacitors

Investigations of the electrode materials used for the capacitors and of the effects of the partial pressure of oxygen present in the vacuum systems during the evaporation of silicon monoxide dielectrics are continuing. Results to date indicate that units fabricated with gold electrodes and with oxygen present in the vacuum system during evaporation of the silicon monoxide produced capacitors with the best life characteristics. A group of 12 units of this type have been fabricated for an aging study of encapsulated gold electrode silicon monoxide capacitors. These units showed a 92% fabrication yield, and consistent leakages for capacitors of equal area.

For optimum results, it is necessary that the substrates onto which silicon monoxide films are deposited be preheated before evaporation. During this reporting period, some experimentation was done with the geometry of the preheater in the vacuum system, in an attempt to obtain more efficient preheating of the substrates. Previously, this preheating was accomplished by suspending a heated metallic strip in close proximity to the back of the substrate, resulting in the substrate becoming hot due to radiated heat from the metallic strip. An attempt was made to place the metallic strip in contact with the back of the substrate in order to obtain more efficient heat transfer, but the resulting film showed evidence of large temperature variations over the substrate during evaporation.

During the next period, life tests will continue on silicon monoxide capacitors with various electrodes and various deposition parameters. In addition, aging and environmental tests of the encapsulated gold electroded capacitors will begin.

The aging and environmental tests initiated on a group of 94 silicon monoxide capacitors during the last reporting period were completed during the current period. An additional quantity of silicon monoxide capacitors with gold electrodes were run following the initial life tests. While the initial tests were run at a temperature of 125°C, the second group of tests was run for 48 hours at 125°C followed by 240 hours at 85°C. All capacitors in both groups were electrically stressed at 12 VDC throughout the tests. The results of these life tests are given in Figure 1. On the basis of these tests, it would appear that encapsulated silicon monoxide capacitors with aluminum electrodes have the most favorable lifetime characteristics.

3.5 Tin Oxide Resistors

During this reporting period, a series of aging studies was performed on a group of tin oxide films deposited on both glazed ceramics and passivated silicon substrates. Aging characteristics of the films at temperatures of 20°C, 60°C, 125°C and 150°C were measured. In the higher temperature ranges, an initial decrease in the sheet resistivity in the tin oxide films was noted, followed by an increase with time to a value higher than the initial resistivity. This aging effect is inversely proportional to film thickness, i.e., the thicker the film the smaller the variation in resistance over a given period of time.

Figure 1

SiO Capacitor Life Test Results

Group 1

Temperature = 125°C
12 VDC applied to capacitors continuously
Test duration = 600 hours

Electrode Material	Capacitor Type	$\bar{M}$	Limits of 95% Confidence Interval	
		hrs	hrs	hrs
Al	Large encapsulated	1240	336	49,600
Al	Large unencapsulated	320	230	529
Al	Small encapsulated	3020	820	120,800
Al	Small unencapsulated	571	260	2,091
Au	Large* encapsulated	166	81	510
Au	Small* encapsulated	2485	674	99,400

Group 2

48 hrs at 125°C followed by
240 hrs at 85°C
12 VDC continuously applied to capacitors

Au	Large* unencapsulated	1422	512	11,800
Au	Small* unencapsulated	3000	813	120,000

$\bar{M}$ = Estimate of mean time to failure based on assumption of a constant failure rate

* Large: Cap. = 350-450 mmf
* Small: Cap. = 25- 35 mmf

The aging results at 20°C showed no discernible trend, the magnitude and direction of change in resistance varying from one film to the next. The most consistent results were obtained from a set of substrates aged at 125°C. Here the direction of resistance change was consistent for all five films with only the magnitude varying with film thickness.

Further investigation in this area is warranted before conclusions can be drawn from the present data.

During the next period the aging stability study will be concluded. An attempt will be made to detect the characteristic resistance (resistivity) vs. time relationship using the aging temperature as a parameter. Further, an effort will be made to define the physical and/or chemical mechanisms involved in the observed aging pattern of these tin oxide films.

Aging studies to date indicate a much higher degree of stability in tin oxide films deposited on SiO_2 passivated silicon wafers compared to those deposited on glazed ceramic substrates.

The aging stability of films deposited on silicon is increased by encapsulation with a TiO_2 film.

Two sets of films were made to conclude the aging study on silicon substrates. The films in the first set were encapsulated immediately after deposition; the second set was aged at 125°C for 24 hours prior to encapsulation. As a whole, the first set of films was only slightly more stable than the second set. (Experimental data are depicted on the accompanying figures. See Figures 2 and 3. It is apparent from a comparison of this data

AGING EFFECTS
ENCAPSULATED LOW TEMPERATURE TIN OXIDE RESISTORS
SUBSTRATE: SiO_2 COATED SILICON
AGING TEMPERATURE: 125°C.

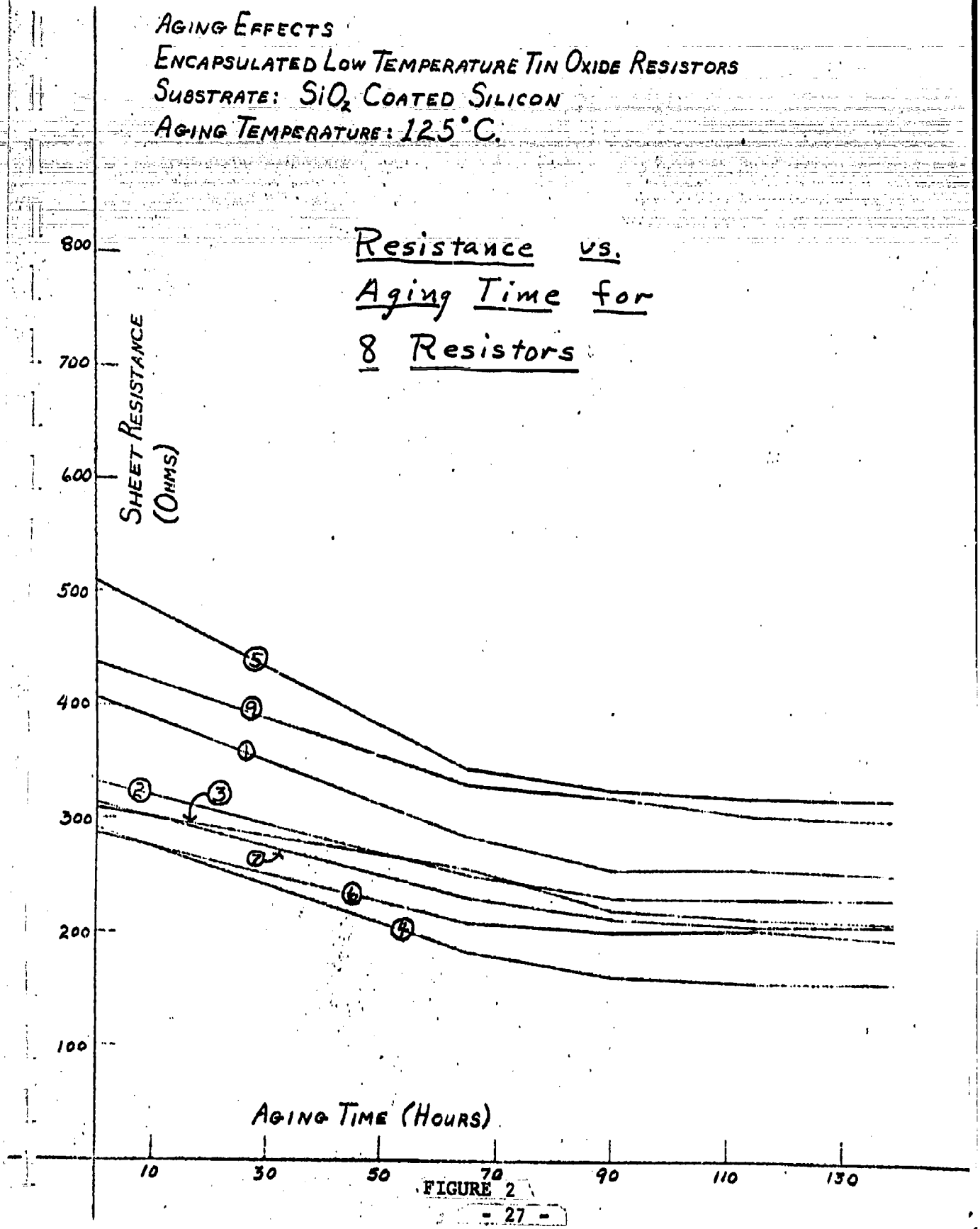


FIGURE 2

AGING EFFECTS
ENCAPSULATED LOW TEMPERATURE TIN OXIDE RESISTORS
AGED 24 HRS. PRIOR TO ENCAPSULATION
SUBSTRATE: SiO_2 COATED SILICON
AGING TEMPERATURE: 125°C.

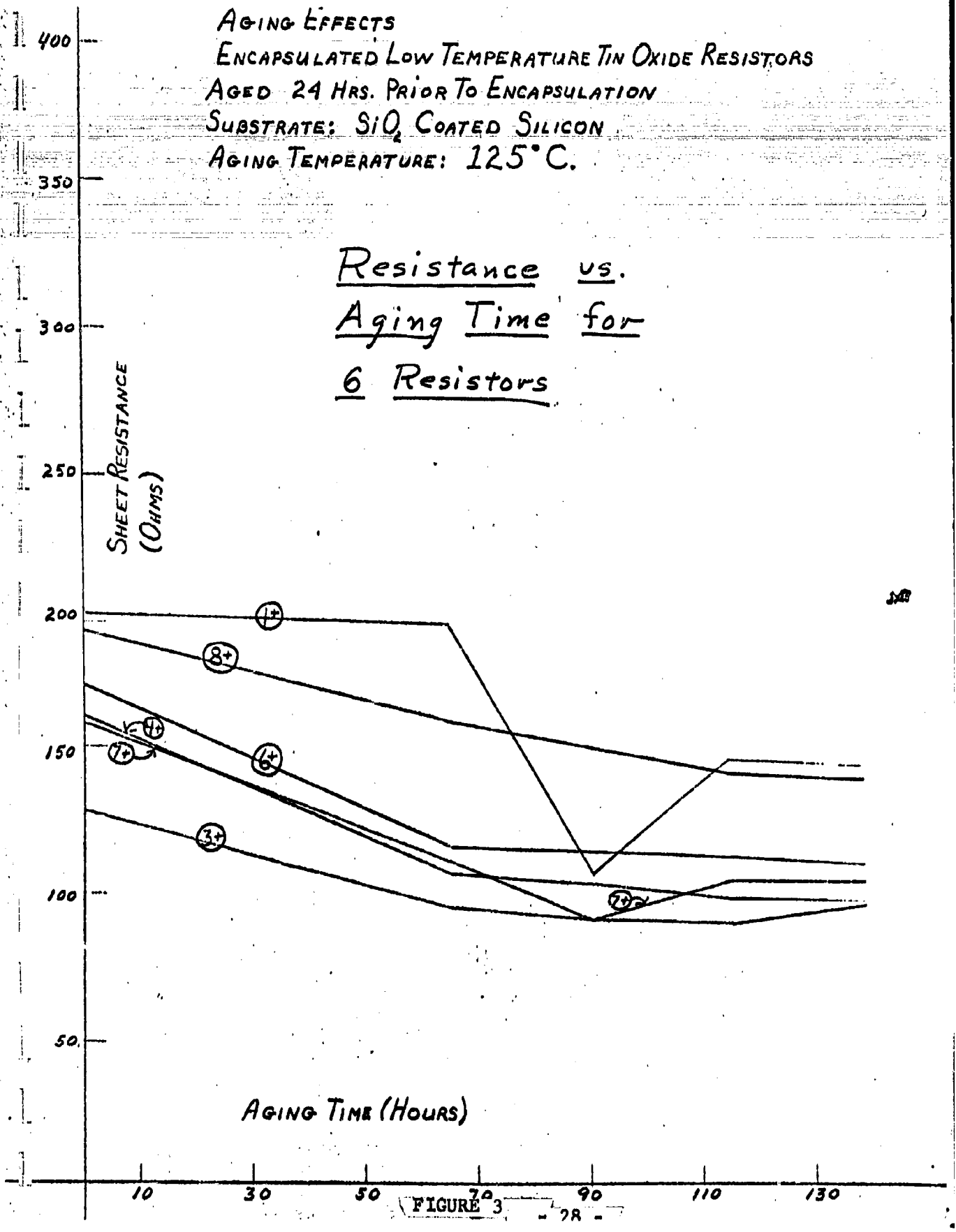


FIGURE 3

that there were anomalous effects involved in the deposition of tin oxide films on a ceramic substrate.

A further aspect of the relative stability of tin oxide on aging that came to light during this study was the effect of encapsulation on the film resistance. All the films used in this experiment showed a decrease in resistance of approximately 10 to 15% upon encapsulation.

The aging studies to date have been made with pure undoped tin oxide films, since the aging characteristics of undoped films provide a sensitive indication of contamination of the films from substrate materials. Resistor films doped with such materials as antimony and indium are expected to have considerably more stable aging characteristics, and will be studied during the following reporting period. (See Figure 5 - 8)

3.6 Interconnection of Integrated Circuit Submodules

Present effort is being directed to three concepts of interconnection.

1) The submodules (functional electronic blocks) are stacked and encapsulated with wires protruding from the edges of the submodule which are cut off flush with the surface of the encapsulant. A process for the low temperature deposition of thick metallic aluminum films is being investigated, which, if successful, will permit an aluminum film to be deposited on the periphery of the encapsulated submodules and photoetched leaving an aluminum conductor between desired points.

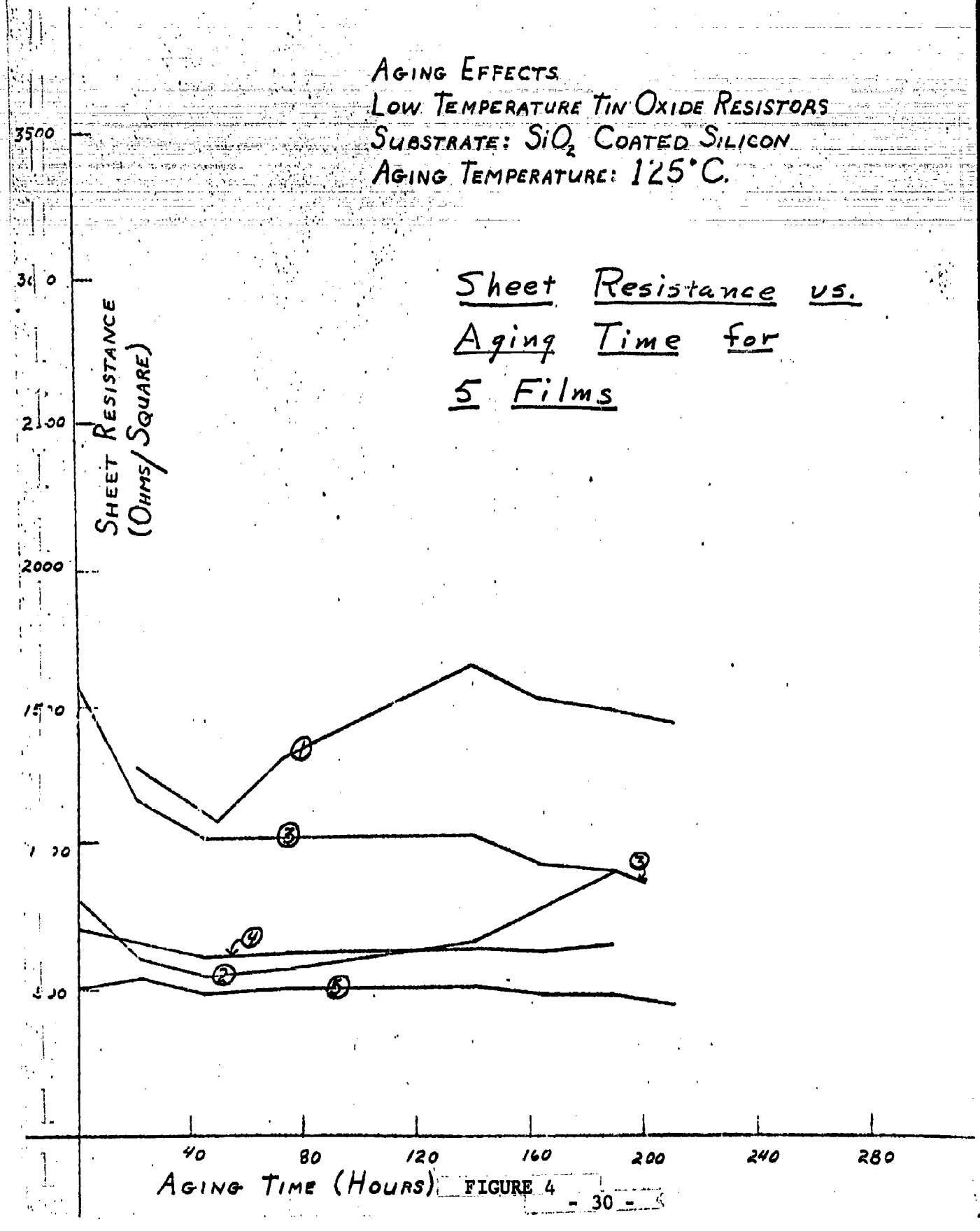

AGING EFFECTS
LOW TEMPERATURE TIN OXIDE RESISTORS
SUBSTRATE: SiO_2 COATED SILICON
AGING TEMPERATURE: 125°C.
Sheet Resistance vs. Aging Time for 5 Films
SHEET RESISTANCE (OHMS/SQUARE)
3500
2000
40
80
120
160
200
240
280
AGING TIME (HOURS)
1
2
3
4
5

FIGURE 4

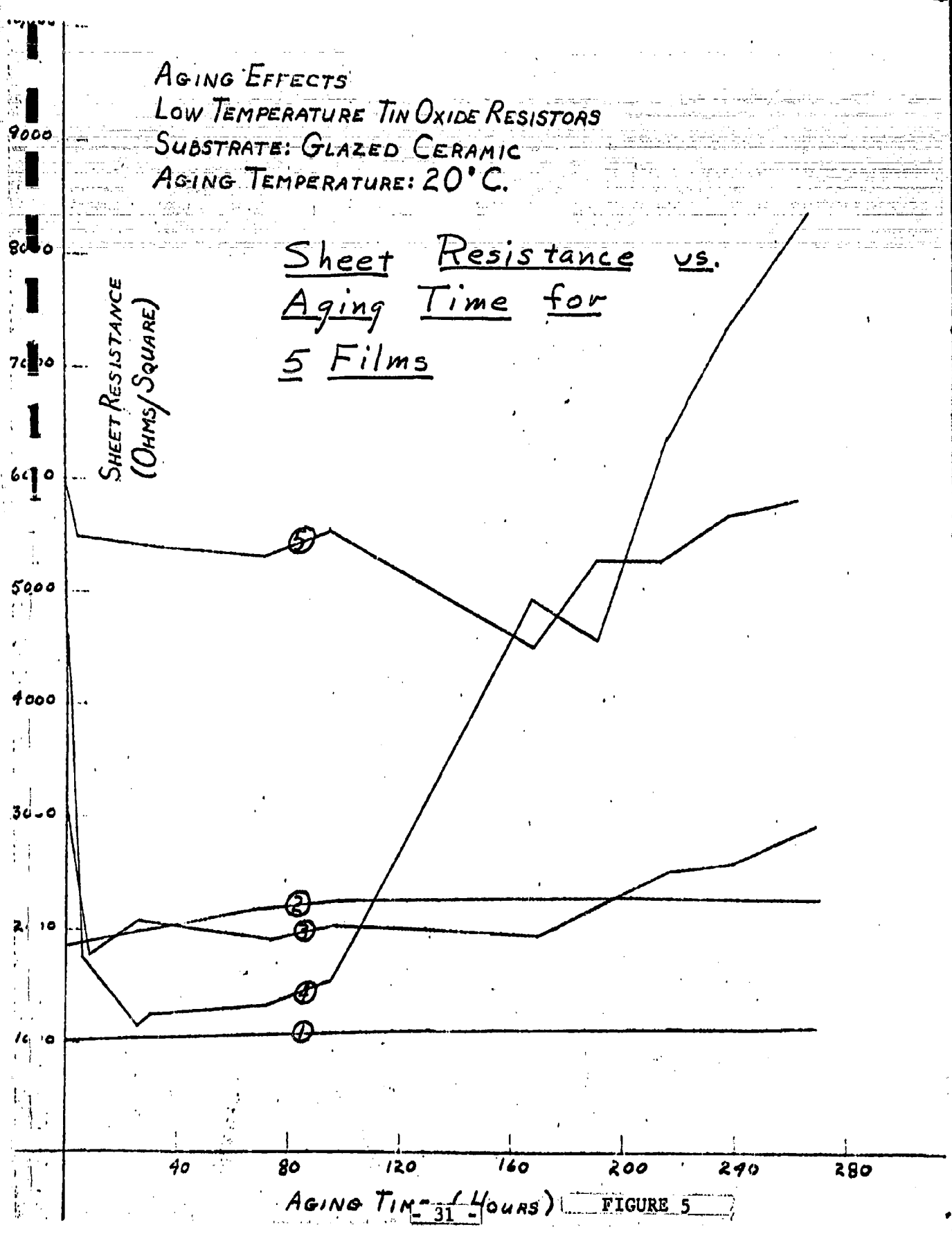

AGING EFFECTS
LOW TEMPERATURE TIN OXIDE RESISTORS
SUBSTRATE: GLAZED CERAMIC
AGING TEMPERATURE: 20°C.
Sheet Resistance vs. Aging Time for 5 Films
SHEET RESISTANCE (OHMS/SQUARE)
9000
5000
4000
40
80
120
160
200
240
280
AGING TIME (HOURS)
1
2
3
4
5

FIGURE 5

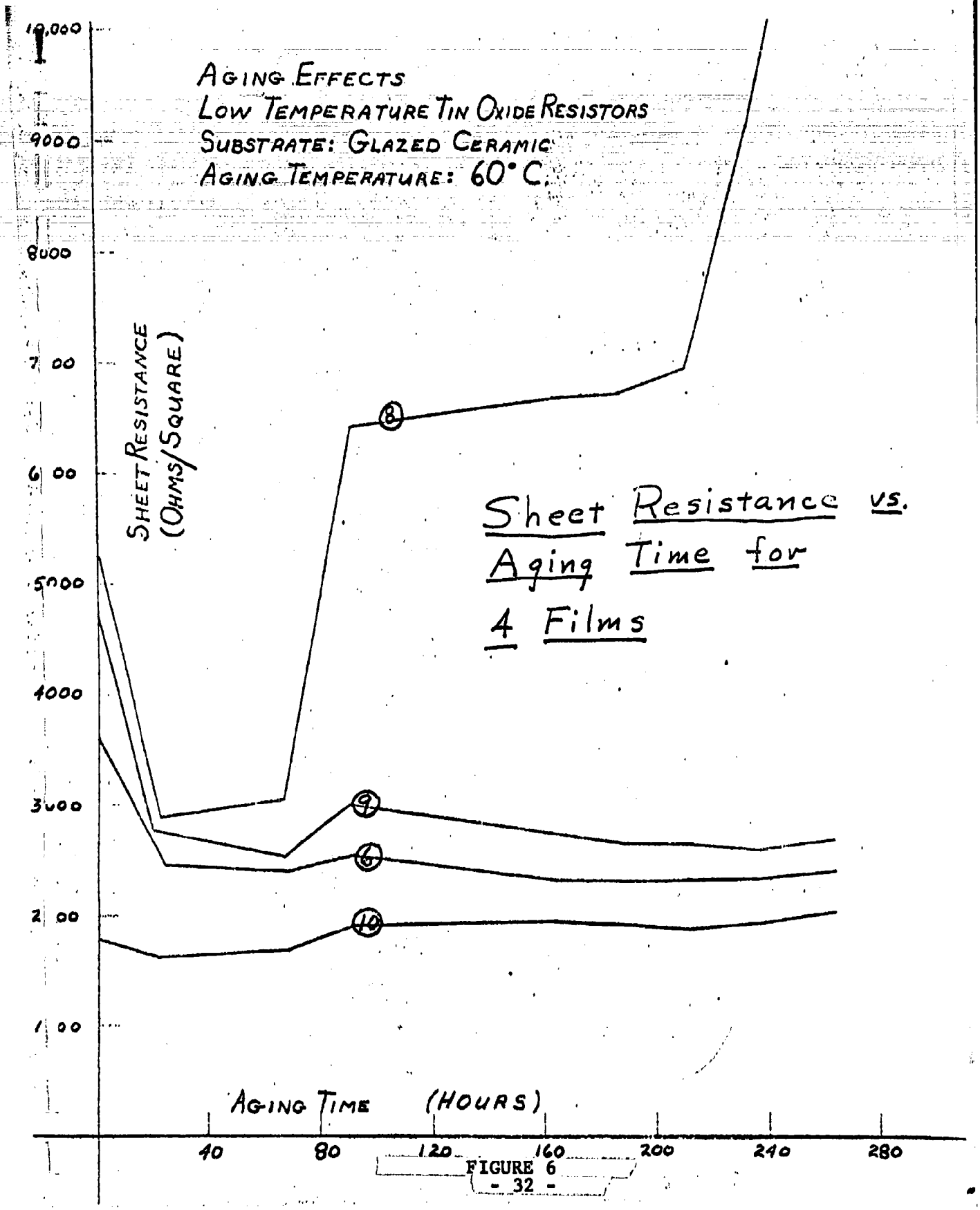

AGING EFFECTS
LOW TEMPERATURE TIN OXIDE RESISTORS
SUBSTRATE: GLAZED CERAMIC
AGING TEMPERATURE: 60° C.
10,000
9000
8000
7 00
6 00
5000
4000
3000
2 00
1 00
SHEET RESISTANCE (OHMS/SQUARE)
8
9
6
10
Sheet Resistance vs. Aging Time for 4 Films
AGING TIME (HOURS)
40
80
120
160
200
240
280

FIGURE 6

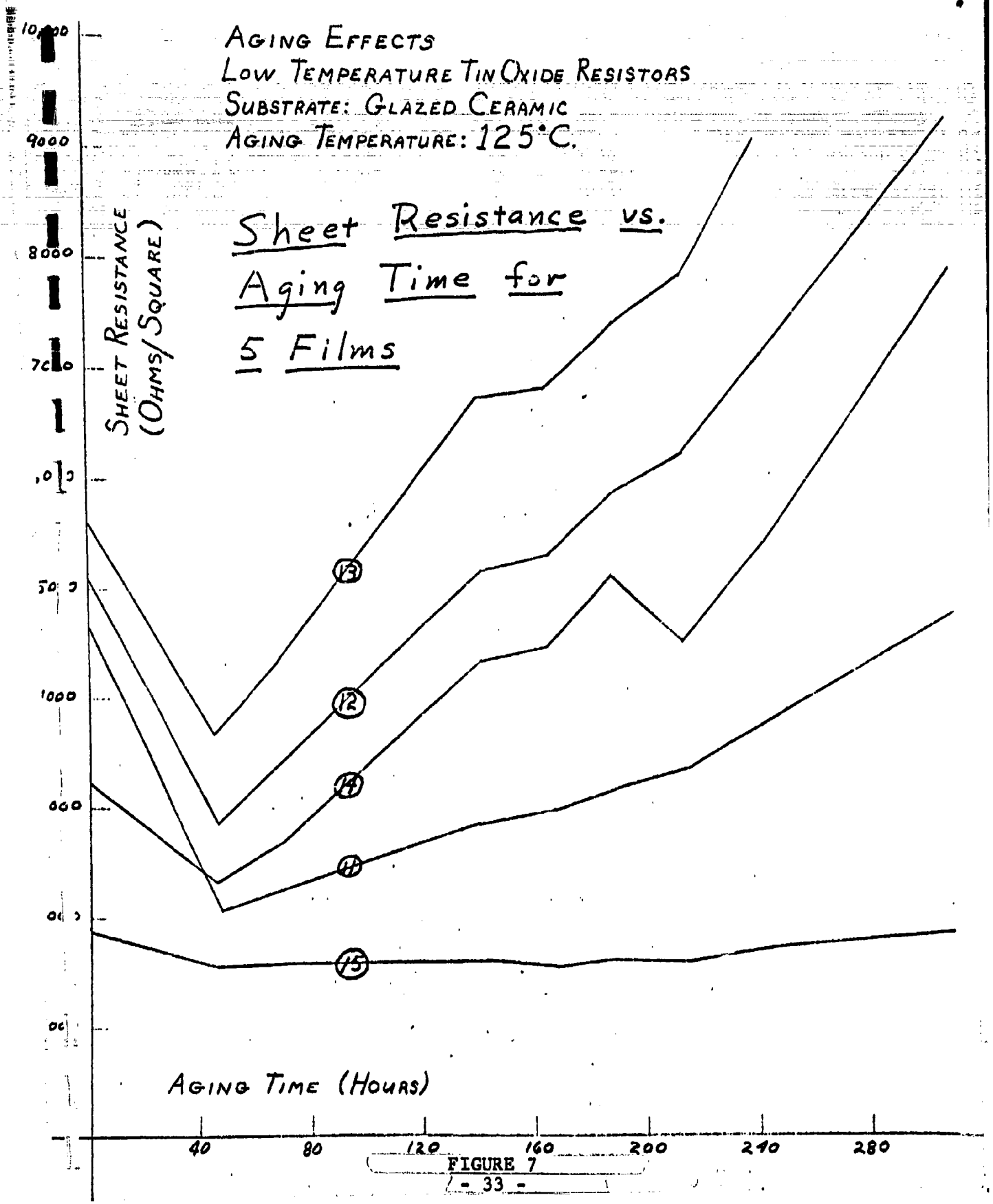

AGING EFFECTS
LOW TEMPERATURE TIN OXIDE RESISTORS
SUBSTRATE: GLAZED CERAMIC
AGING TEMPERATURE: 125°C.
Sheet Resistance vs. Aging Time for 5 Films
SHEET RESISTANCE (OHMS/SQUARE)
9000
8000
1000
AGING TIME (HOURS)
40
80
120
160
200
240
280
13
12
14
11
15

FIGURE 7

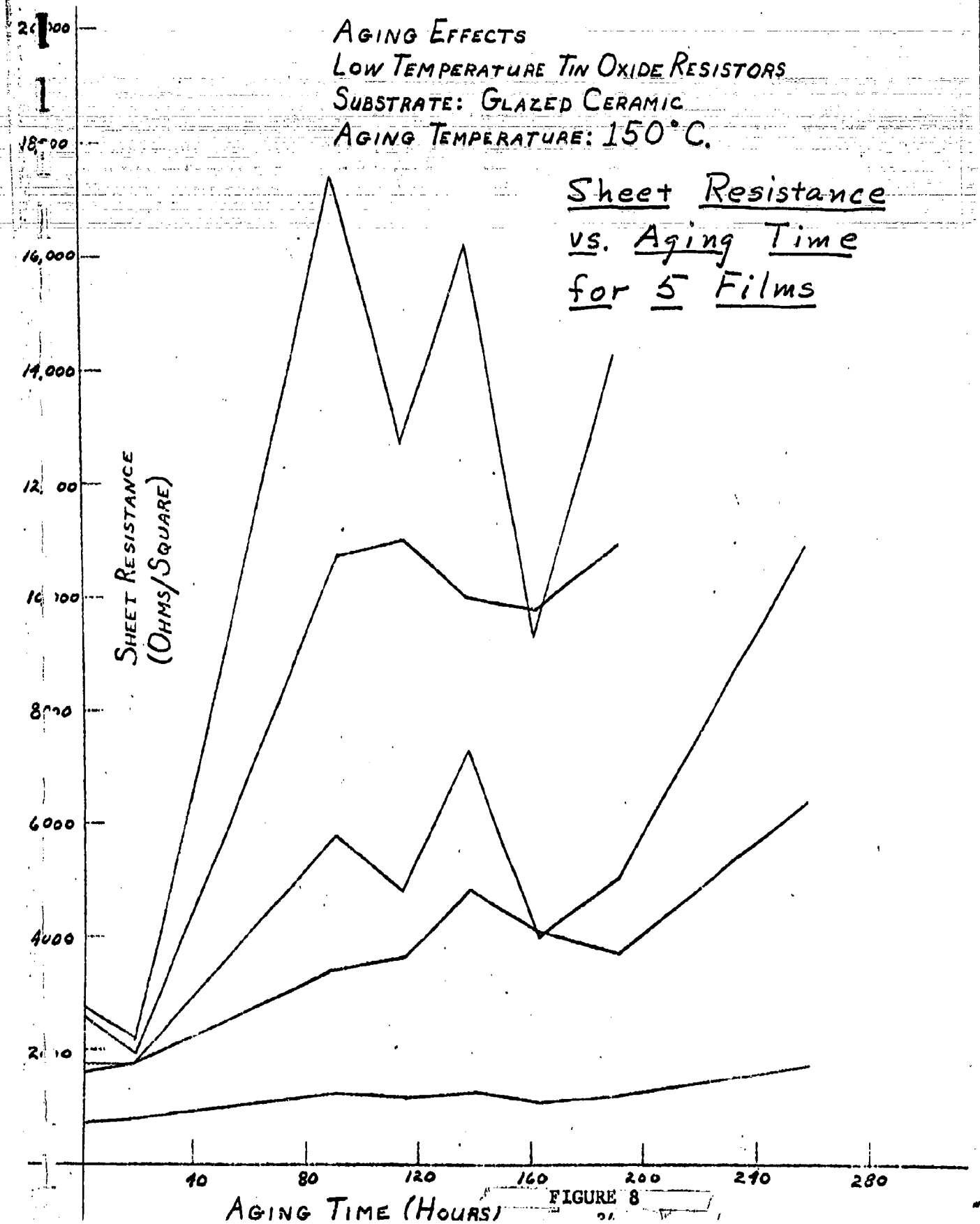

AGING EFFECTS
LOW TEMPERATURE TIN OXIDE RESISTORS
SUBSTRATE: GLAZED CERAMIC
AGING TEMPERATURE: 150°C.
Sheet Resistance vs. Aging Time for 5 Films
SHEET RESISTANCE (OHMS/SQUARE)
16,000
14,000
6000
4000
40
80
120
160
200
240
280
AGING TIME (HOURS)

FIGURE 8

2) The submodules are stacked and encapsulated as in the previous concept, but connections are made by the use of metallic foil conductors.

3) The submodules would be mounted on multi-layered etched circuits boards.

A procedure for depositing thin aluminum films by pyrolsis reaction is currently under investigation.

In order to evaluate the usefulness of the aluminum films as means of obtaining satisfactory interconnections between submodules, a module consisting of six submodules stacked with test thin film components is now available to attempt interconnection by this process. The basic requirements for a substrate material have not been firmly established. Therefore, modification to the present module may be necessary once the parameters are firm. The basic plan for this concept is to deposit the aluminum on one surface having perhaps as many as 36 contacts. The desired pattern of interconnection will be masked off and the exposed aluminum etched away. Multilayered interconnections can be accomplished by coating each conductor layer with a dielectric film and subsequently depositing aluminum over the dielectric film repeating the above process.

The metallic foil conductor process is similar to the above with the exception of the technique of laying down the foil. The foil is applied against a "B" staged film adhesive between contacts by a hot stamping process. The contacts are then connected to the foil by an ultrasonic welding process. Preliminary attempts to determine feasibility have been only moderately successful.

The foil was applied to the module, etched, and removal was attempted by immersion in an ultrasonic cleaning tank. The remaining conductor, however, was not uniform in width and had very ragged edges. New techniques are currently under study.

Interconnection by a multilayered etched circuit board is being investigated. The artwork for a prototype board is now in the layout stage.

4.0 SILICON PROCESS AND INTEGRATED CIRCUIT TECHNOLOGY

4.1 Epitaxial Diffused Integrated Circuits

4.1.1 Optimized Structure for Integrated Circuits

The attempts at reducing series collector resistance are continuing and showing progress. The method being used was discussed in the monthly status report for April 1962. A heavily-doped planar N-type layer is diffused into a P-type substrate. The original and regrown silicon dioxides are then removed and an N-type epitaxial layer is grown over the entire wafer. A silicon dioxide layer is regrown and the pattern for the isolating P-type grid is formed in this oxide layer. A P-type diffusion through the N-type epitaxial layer is performed. A photograph of a device after the epitaxial growth step is shown in Figure 1. Figures 2 through 9 illustrate a series of cross-sectional views of a wafer similar to that shown in Figure 1. Figure 7 shows the depth of penetration of the N-type layer (white) into the P-type substrate (dark region). The gross white area is the N-type epitaxial layer The registration of the N-type diffused layer to the trace pattern left on the surface after epitaxial growth is quite good.

A group of NAND-NOR logic circuits has been processed through the step shown in Figure 10.

Another group of circuits expressly designed for testing the optimized structure have been processed up to the epitaxial growth operation. These circuits are shown schematically in Figures 11 and 12.

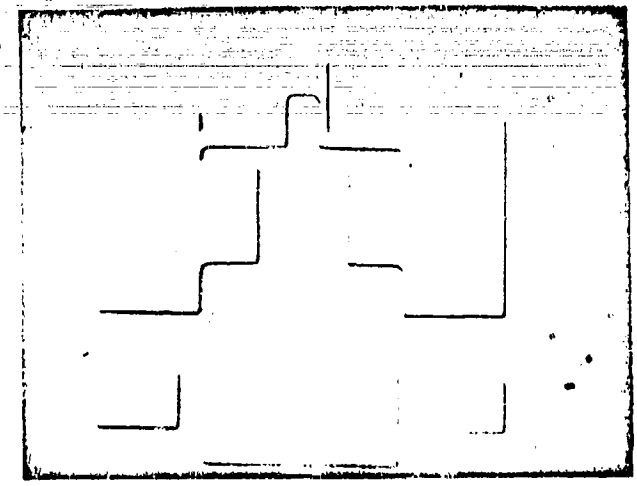


FIGURE 1

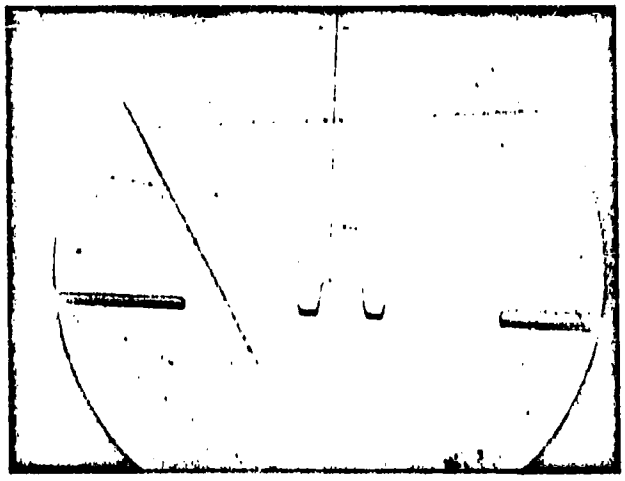


FIGURE 2

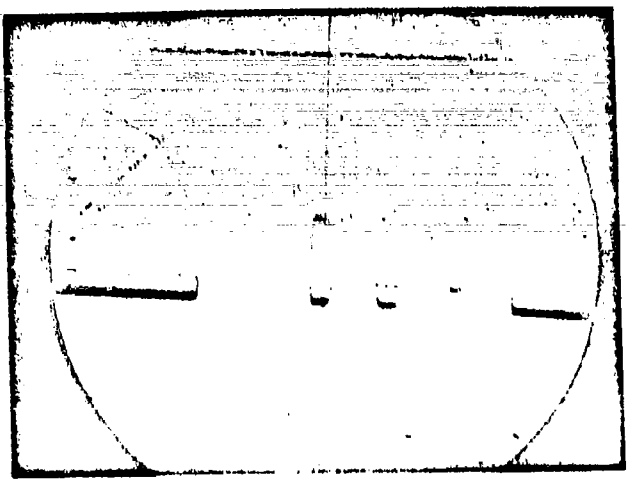


FIGURE 3

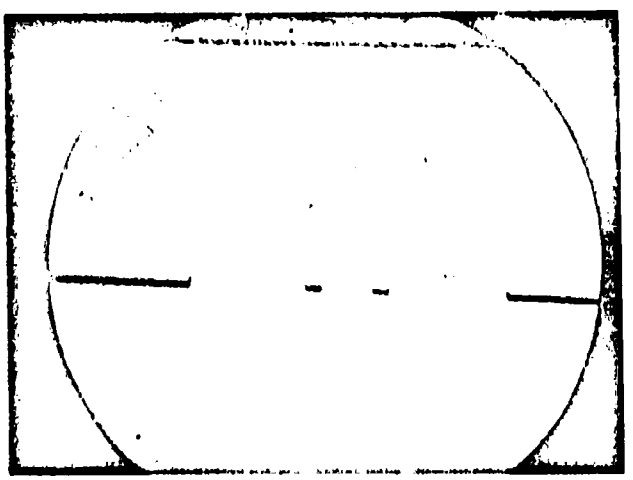


FIGURE 4

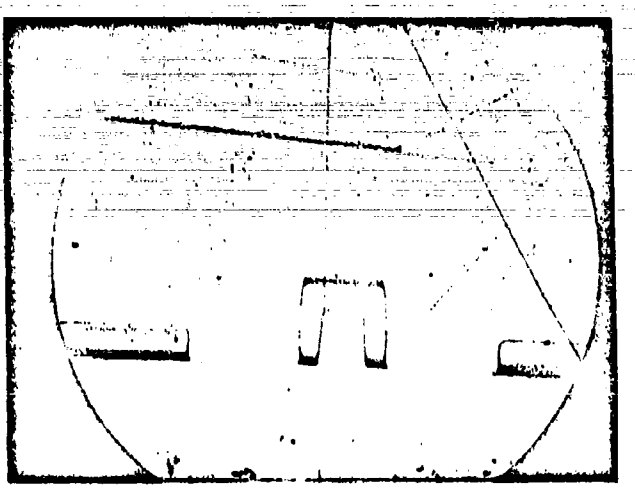


FIGURE 5

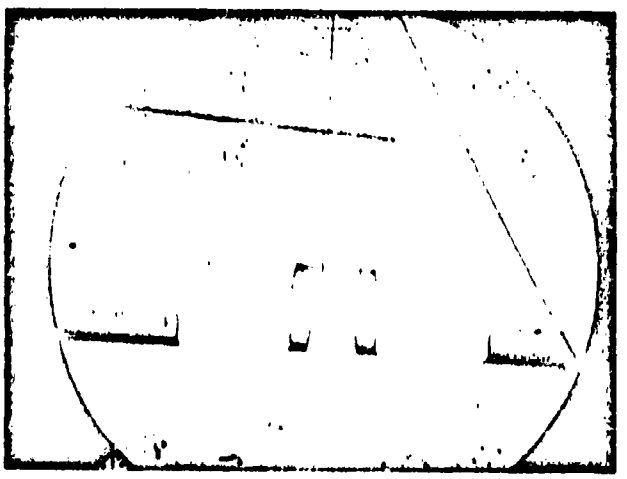


FIGURE 6

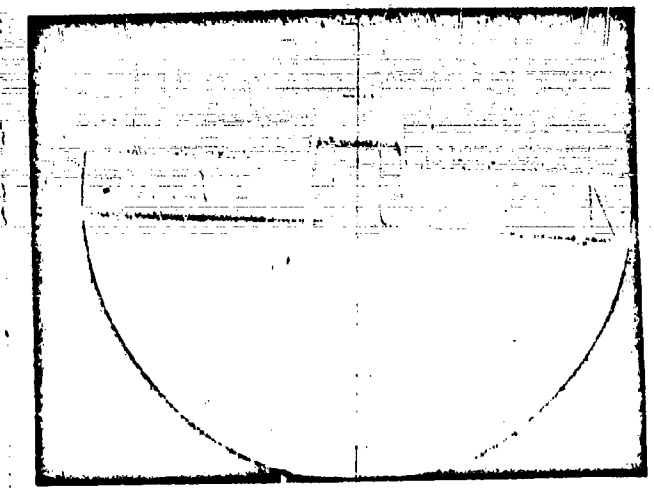


FIGURE 7

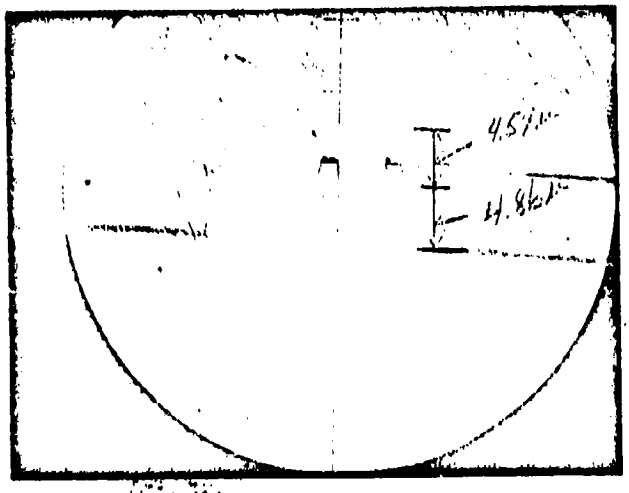


FIGURE 8

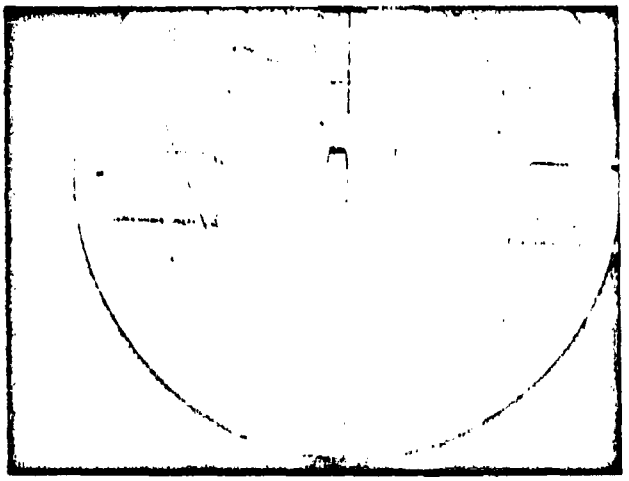
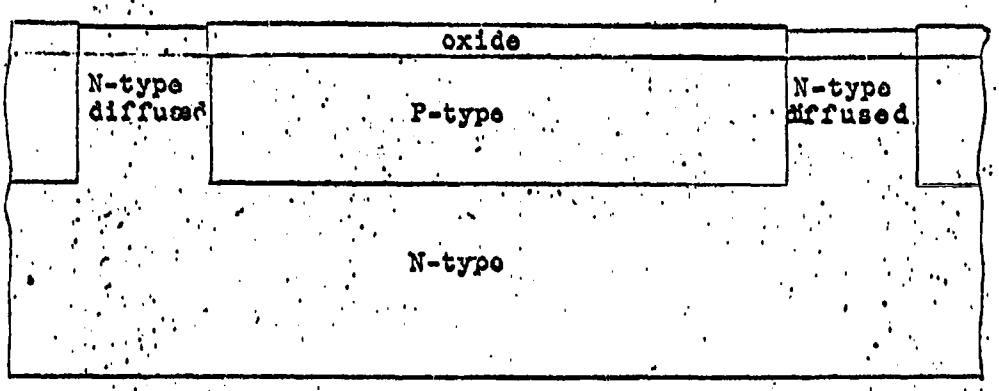


FIGURE 9

-- Diffusion of isolation channels



Base diffusion

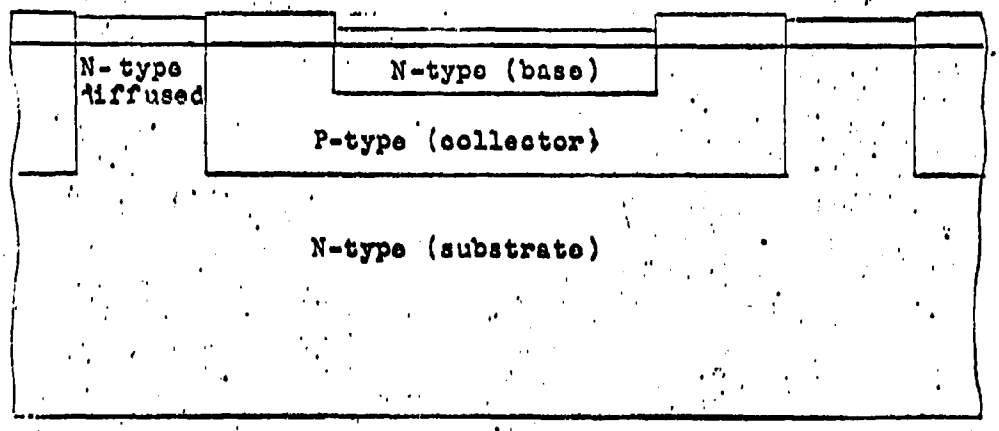
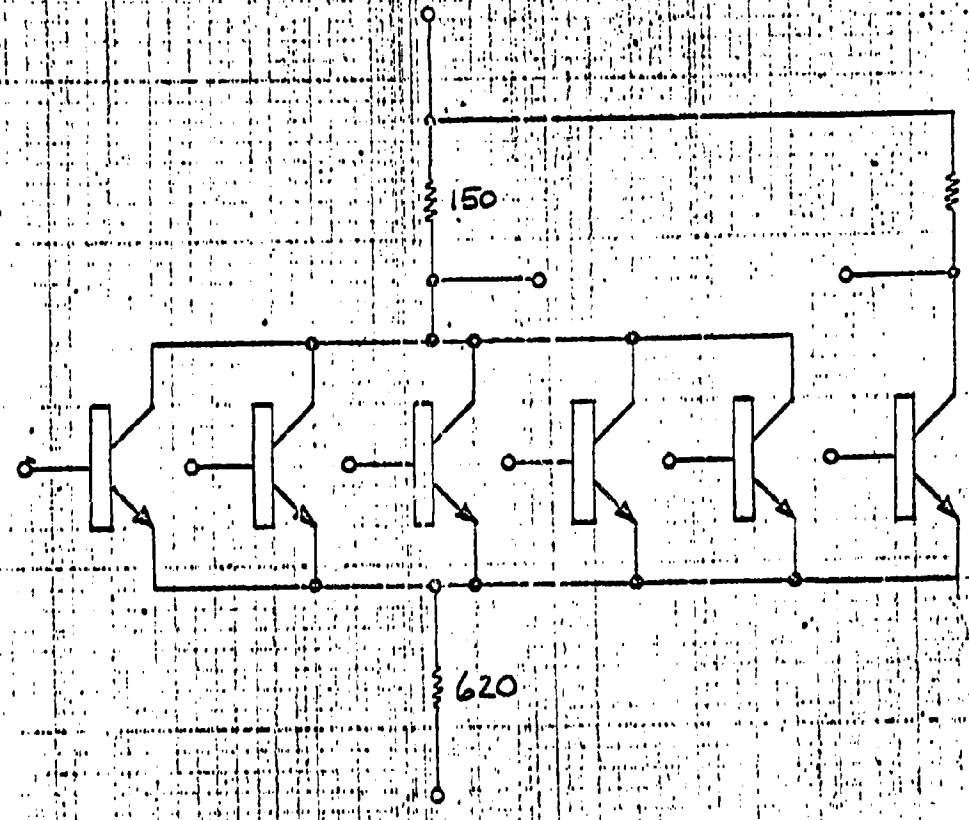


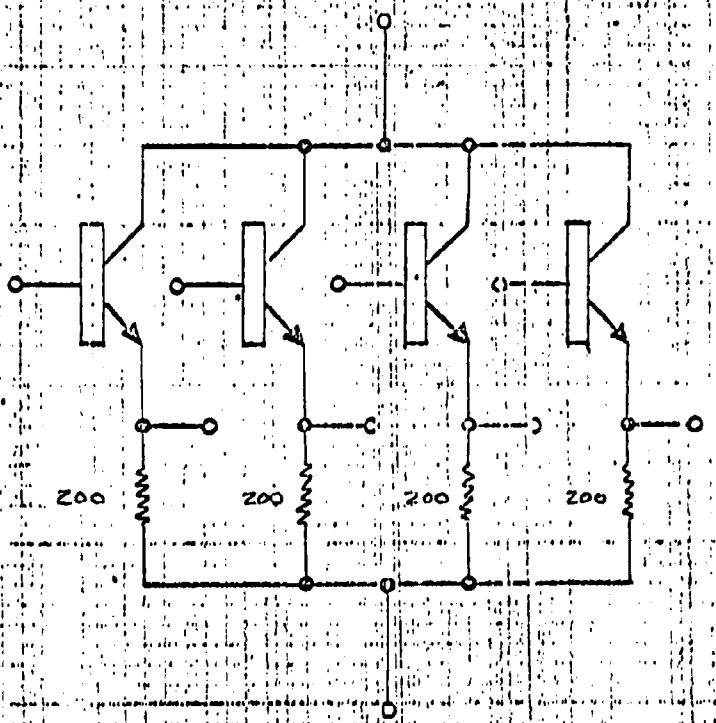
FIGURE 10



MECL - OR/NOR

5/4/82 DSK

FIGURE 11



MECL Translator

5/4/82 DSK

FIGURE 12

4.1.2 PNP Integrated Circuits

All attempts to make silicon integrated circuits in the past have been limited to those using the NPN transistors as the basic device. Work has been initiated on integrated circuits using the PNP transistor structure.

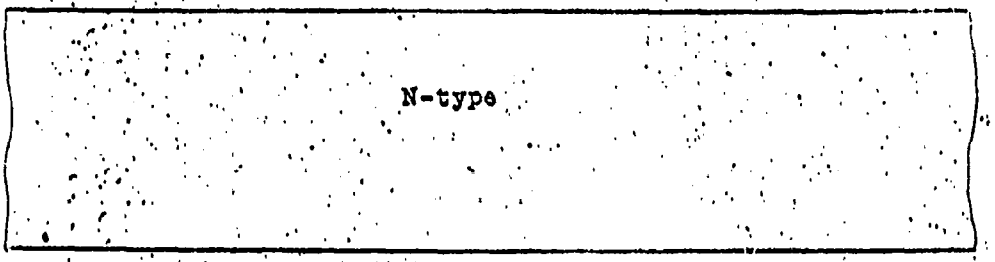
The geometry to be used as a test vehicle in this program will be the same high frequency transistor as used in the NPN circuit development. The PNP silicon transistor presents a large list of problem areas which will have to be resolved. However, the basic scheme of isolation to be used in the PNP circuits is similar to that used in the NPN circuits.

The sequence of operations to be employed in the fabrication of the PNP circuits is illustrated in Figures 13, 14 and 15.

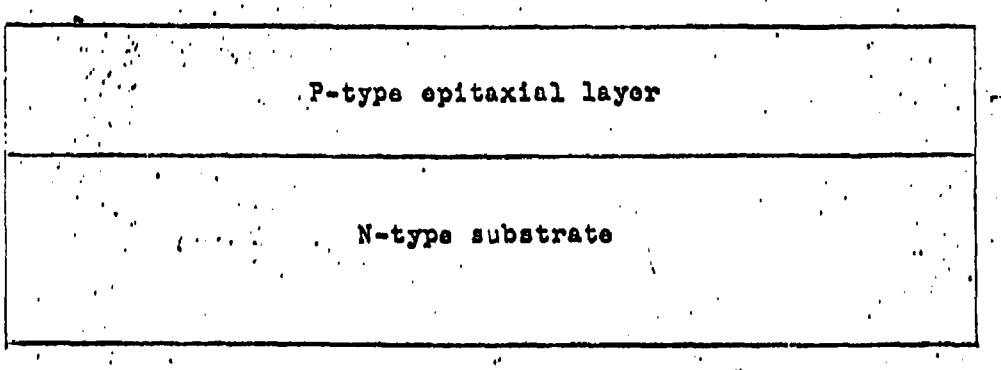
High resistivity N-type silicon is used as the starting material. On this N-type substrate, a P-type epitaxial layer of approximately one ohm-cm resistivity and a thickness of 20 microns is grown upon the N-type substrate. An oxide layer is grown upon the P-type epitaxial layer. The pattern for the isolating N-type grid is formed in this oxide layer, and an N-type channel is diffused through the P-type epitaxial layer to the N-type substrate.

The pattern for the N-type base diffused region is formed in the original oxide layer, and an N-type region is diffused into the P-type epitaxial layer. The junction depth will be approximately 2.8 microns, and the surface concentration

Cross-sectional view of integrated circuit structure using PNP transistors



Epitaxial collector growth



Initial oxidation

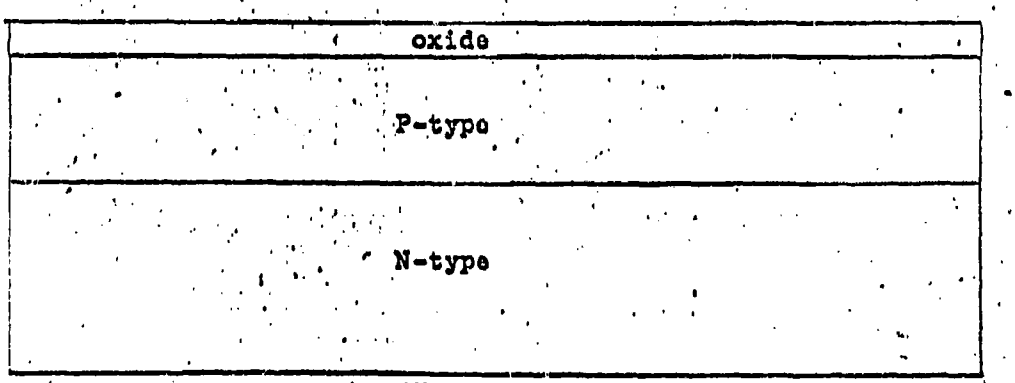
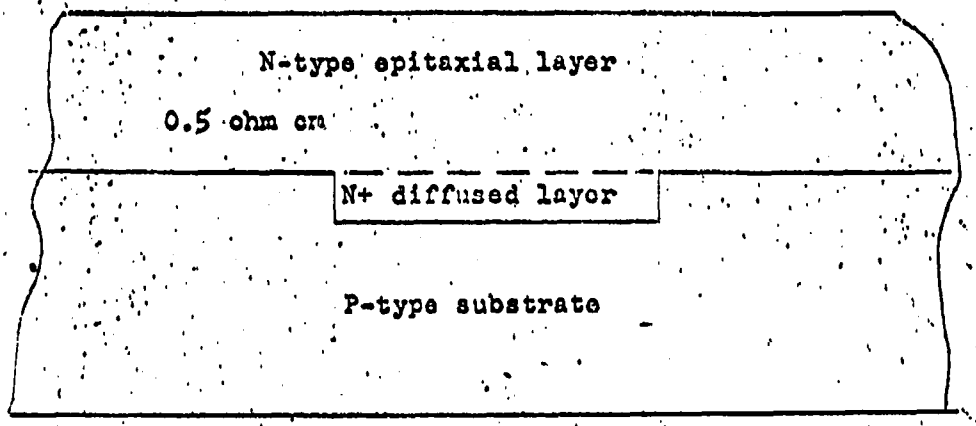
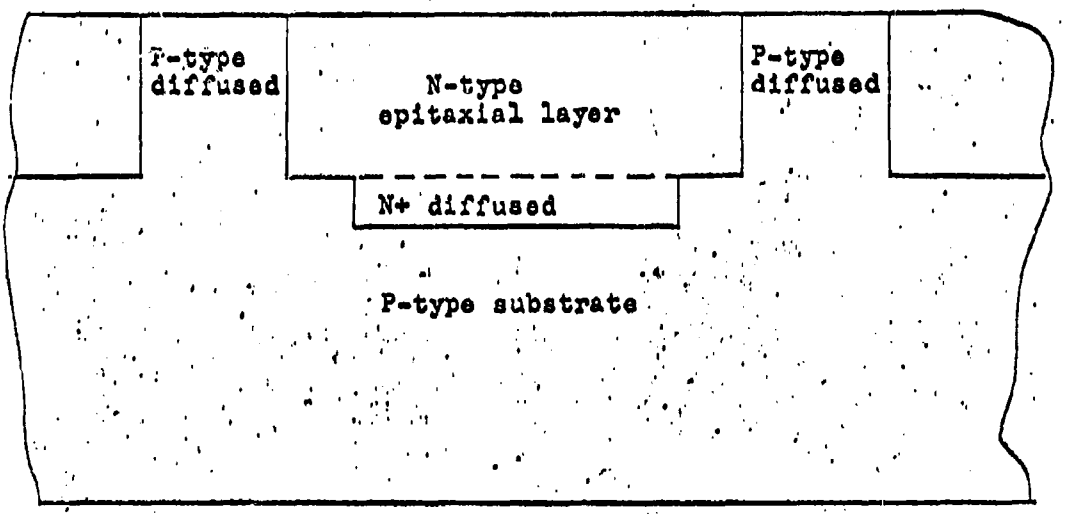


FIGURE 13



(a)

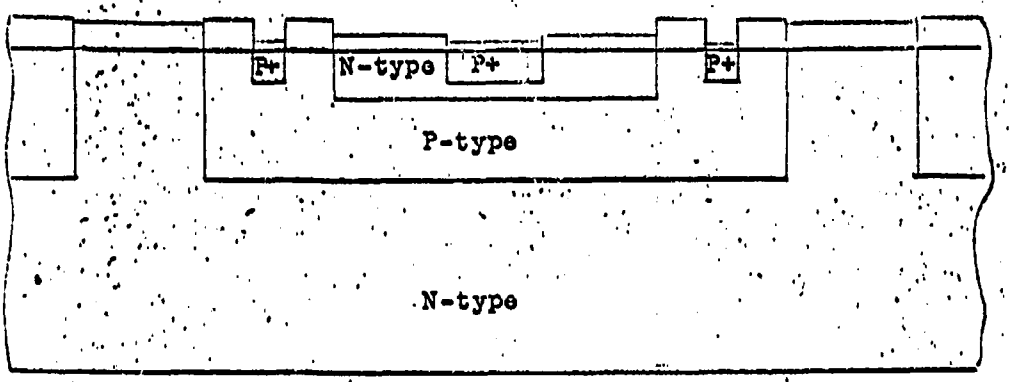


(b)

Cross sectional view of optimized integrated circuit structure

FIGURE 14

Emitter diffusion



Metalized circuit
ohmic contacts

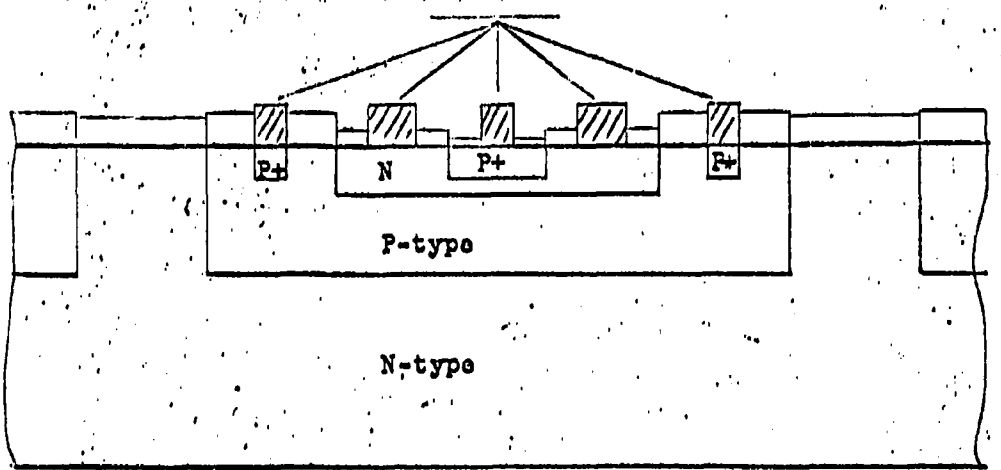


FIGURE 15

Degenerate N+ region formed in base region in PNP transistors

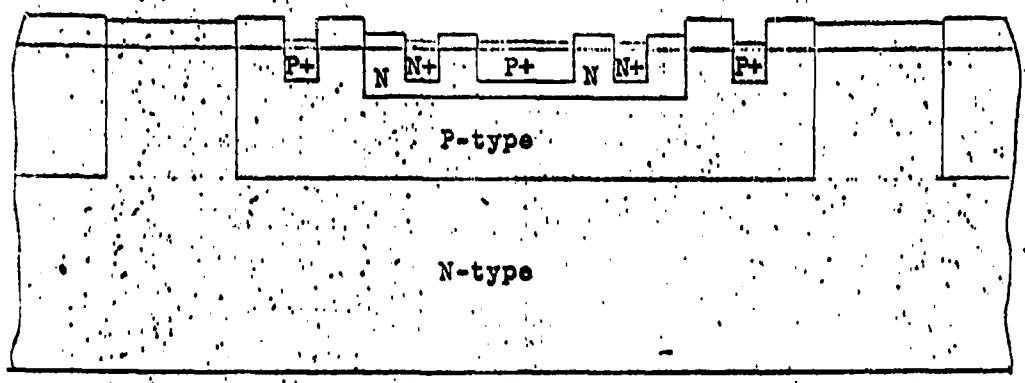


FIGURE 16

will be in the vicinity of 10^{18} atom/CC. An oxide layer is regrown over the base region during the diffusion operation. The pattern for the P-type emitter is formed over the N-type base region, and a boron diffusion is performed such that a base width of one micron or less is obtained.

At this point, the wafer is ready for an ohmic contact oxide etching operation. However, the problem of forming ohmic contacts with aluminum on N-type silicon once again arises. Aluminum dopes silicon to approximately 2×10^{19} atoms/CC when alloyed. The base region is doped to 10^{18} atoms/CC (N-type). If the aluminum is alloyed to the base region such that a "regrowth" layer of aluminum-doped single crystal silicon is formed, the contact on the base region will be rectifying, not ohmic.

Therefore, a degenerate N+ region must be formed in the base region, as is shown in Figure 16.

The masks required to perform all these operations have been obtained, and groups of wafers have been processed through the isolation channel diffusion.

4.2 Bonding Reliability Studies

Measurements have been taken on 11 SiO_2 capacitors, which have completed a storage life test of 1000 hours at 300°C. The capacitors were the SiO_2 type with aluminum metallization. Aluminum wire, .007" diameter, was bonded between the metallization pattern and the gold plated post of the header.

The primary purpose of this test was to determine the effect of high temperature on the aluminum to aluminum bond.

Normal techniques which bond gold wire to aluminum metallization are not reliable after long periods above 300°C. The results of this test are shown in Table 1.

After 1000 hours, units #6 and #7 were open. Later inspection indicated that the Al. to Au bond at the post was open while the Al. to Al. bond on the unit was good. These results indicate that an all aluminum system would be more reliable after high temperature storage. Devices of this type are now being constructed for testing.

Bonding Reliability Studies

	Hours	
Unit	0	1000
1	33	32
2	38	35
3	35	34
4	33	32
5	35	33
6	35	Open
7	34	Open
8	32	30
9	29	28
10	23	23
11	33	32

Capacitance Value in pf.

TABLE 1

4.3 Diffused Resistor Temperature Coefficients

As discussed previously, the hole mobility in the diffused area is the primary temperature dependent variable in the determination of the total resistance. The slope and magnitude of this temperature dependence is a direct function of the hole impurity concentration. Because the "ohms/sq." value of any diffused area is also a direct function of the impurity concentration and the mobility, the temperature coefficient of the unit becomes a function of the "ohms/sq." This relationship is shown in Figure 17.

As indicated by theory and as shown in the above figure, the temperature coefficient of a diffused resistor decreases with increasing impurity concentration. A useful value of resistivity is then in the range of 100Ω/sq, which results in a temperature coefficient of approximately 1500 ppm. Most integrated devices are now being designed using this value.

Figure 18 illustrated the uniformity of temperature coefficients for three 20 KΩ resistors. At 200Ω/sq., these units had a T.C. of approximately 2300 ppm. The fall-off of the one unit at high temperature was probably due to junction leakage.

4.4 Metallization

A method of connection and interconnection of the elements in integrated circuits. The immediate program is to provide an interconnection of conducting paths between circuit elements which takes advantage of both intrinsic and extrinsic paths. Metallization refers to the system and process of producing

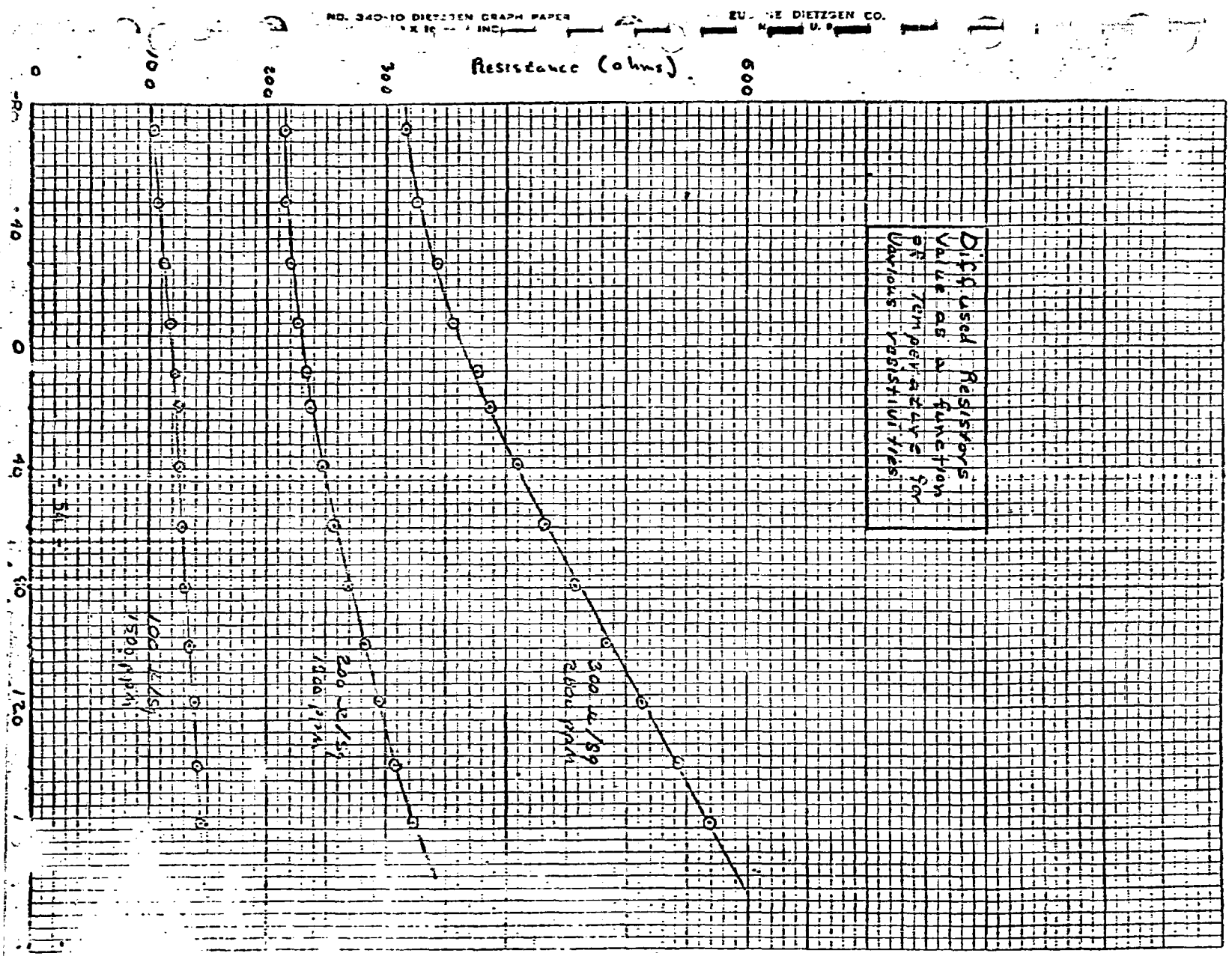

NO. 340-10 DIETZGEN GRAPH PAPER
EUGENE DIETZGEN CO.
Resistance (ohms)
0
100
200
300
500
-40
0
40
80
120
Diff. used Resistors
Value as a function
of Temperature for
various resistivities
-54
100 Ω/sq
200 Ω/sq
300 Ω/sq

FIGURE 17

40K
30K
20K
10K
0
Resistance (Ω)
-80
-40
0
40
80
120
160
200
2300 ppm
Resistance Value vs. Temperature
200 Ω/Sq. Nichrome
Resistors
55

FIGURE 18

the desired extrinsic interconnections. This metallized pattern is to function both for interconnection of elements upon a specific silicon chip and to provide means whereby connection can be secured to the circuit environment.

In lieu of a more refined system with its subsequent and necessary development time and in an endeavor to obtain information of circuit function at an earlier date the following metallizing scheme was envisioned and attempted. The method entailed a metallic pattern formed by photographic techniques and provides contact islands to which thermocompression bonding techniques could then connect to mounting assemblies such as headers.

In detail then, the wafer is prepared by conventional diffusion and epitaxial processes to fabricate the active and passive elements necessary for circuit function. After such a procedure in general, the wafer and all elements are over-laid with an isolating or passivating glass. Appropriate holes are then chemically cut through the glass, utilizing photographic techniques.

The wafer was then introduced into a high vacuum evaporator and aluminum was deposited over the total surface to an estimated thickness of the order of 3000Å. The vacuum deposition was to a substrate whose temperature was not deliberately alleviated in any outgassing procedure.

After deposition, the wafers were "photoresisted" and etched to provide the required interconnection pattern. The photoresist prevents etching where metallization is required.

Subsequently, the operational chips are mounted and connections to outer terminals accomplished via thermal compression bonding to the bonding islands provided in the pattern for this purpose.

Using the above procedure, problems began to emerge and as the problem was investigated, other problems revealed themselves. The prime problem manifested itself in electrical discontinuities (opens) in the interconnecting metallization pattern. See Figure 19.

The opens upon probing always occurred at a "glass step", that is in a region where the metal connector stripe was overlaid upon a change of altitude of the passivating glass, i.e. from the collector ohmic contact window to the bonding island upon the passivation glass There is a change of evaluation of 7,000 -25,000Å depending upon fabrication and the specific structure under consideration. Investigation of this problem led to a number of contributing factors listed below:

(1) Poor adhesion of the photoresists to the deposited aluminum. See Figure 20.
(2) Pin holes in the photoresist.
(3) Poor adhesion of the Al to the glass substrate.
(4) An abundant evolution of gas from the etching reaction which aggravated the emulsion lifting problem.
(5) Large steps and severe surface gradients.

A number of changes were introduced into the metallization process aimed at a solution to the above problems. As a

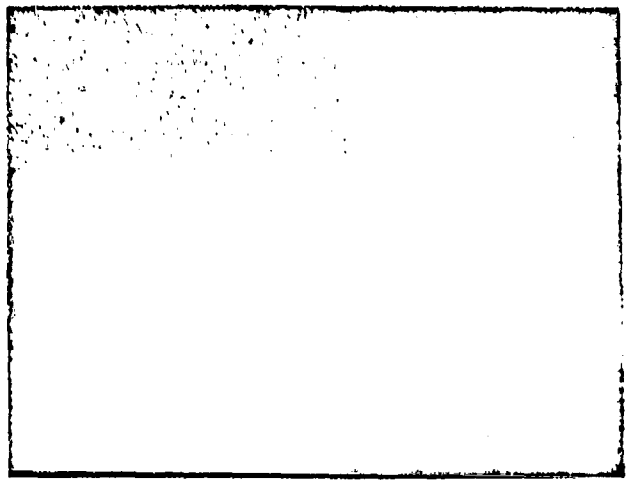


FIGURE 19

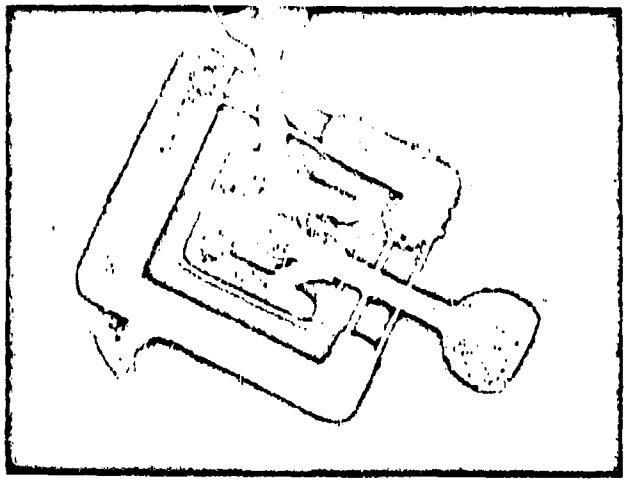


FIGURE 20

consequence, the process in detail is more elaborate, however, this is justified in the greatly improved results which have been obtained to date. Most of the problems which appeared are well in hand or have been virtually eliminated. The only remaining problem is the severe gradient in the glass topography; even here the method while lacking elegance is an adequate one.

The current process is outlined below and a brief discussion of the pertinent changes and their relationship to the above listed problems is included.

In essence, the general procedure is as outlined before, that is the metallizing is vacuum deposited in a continuous strata, selectively etched to produce the desired interconnection pattern. In detail, however, there are a number of changes.

First of all, the wafers are outgassed in high vacuum at high temperatures, secondly, the Al is deposited upon an elevated temperature substrate. These two modifications of the process are introduced to enhance the adhesion of the Al to the silicon and glass surfaces. Quantitative numbers are not available, but the Al adherence is reflected, in that the deposited layer can easily survive the difficult scotch-tape test.

The third innovation is a passivation of the deposited metallic layer in atmosphere at elevated temperatures. The function achieved here is greater adhesion of the photoresist emulsions during the subsequent etching phase of the process.

The fourth change has been in the photo emulsion itself, KPR has been used heretofore, primarily, because of its property

of being readily removed from the remaining pattern after the etching has been achieved. KPR is known for its pin holing difficulties, hence other photo emulsions were investigated.

It has been found that KMER could be removed adequately, provided sufficient care is exercised in the photoresistive preparation. Thus, with an emulsion change, the pin holing problem has been alleviated, further since KMER is an acid resistant preparation and, because of the vigorous reaction of caustic etches alternate etching preparations were given consideration.

The fifth modification involves the etching preparation. We have changed from a vigorour caustic etchant to a milder acid etch. The quantity of gaseous hydrogen evolved is reduced and thus aids uniform etching. This seemingly of little significant fact is essential when time of etching is of sufficient duration to degrade the integrity of the protective emulsion.

The sum total of the above changes is an interconnecting pattern of very fine resolution. See Figure 21. In so doing, the severe under-cutting of the pattern at a "glass step" is virtually eliminated. See Figure 22.

4.4.1 Contact Studies

As mentioned in previous reports, fabrication of contact plates (or tabs) via photo-etching techniques have been achieved. Since then, a metallization has been achieved in the configuration also outlined at that time. Solderability of the contacting photo to this pattern has been attempted, using

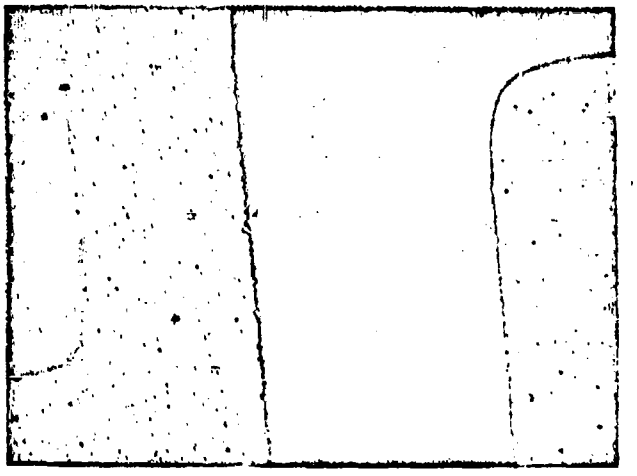


FIGURE 21

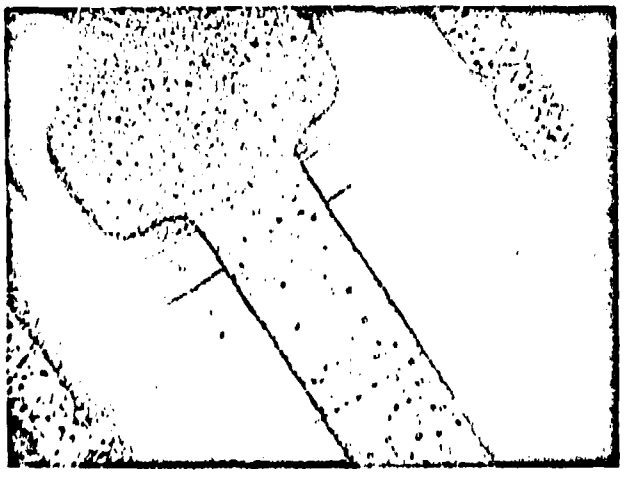


FIGURE 22

solders which have greater than 350°C melting points. Optimization of pressures and quantities of solders have not been yet achieved. However, soldering appears feasible. See Figure 23. Yield and reliability are, as yet, undetermined. Mechanical problems have arisen to how best to separate the interconnected pins without transmitting serious vertical stress to the contacting pattern. Some difficulty has thus far been experienced in the pattern lifting from the glass. It has not yet been determined whether the metal to glass adhesion was poor or whether the stress transmitted was just too great. More work is anticipated in this area.

The details of the etching and evaporating process of the aluminum metallizing was outlined in detail in the previous monthly report. A considerable number of wafers have been processed by the technique and, in general, the results are gratifying. A "bug" appeared in a rather specific case and analysis of the situation led to a slight modification of the operation, this modification appears to have corrected the situation.

It was noted that in a certain circuit pattern which had been processed within the glass etching phases in a manner which deviated from the routine method that these wafers had virtually 100% opens somewhere within the circuit. Further study revealed that all opens within a wafer had the common feature of being oriented relative to the evaporation filament source. Introduction of a rather distributed source for the metal vapors such that the metal in transport came down upon the substrate in a random fashion has reduced this problem. It should be noted that the problem might not have occurred at all, except for the process deviation. However, to insure safety of processing the conservative step was taken.

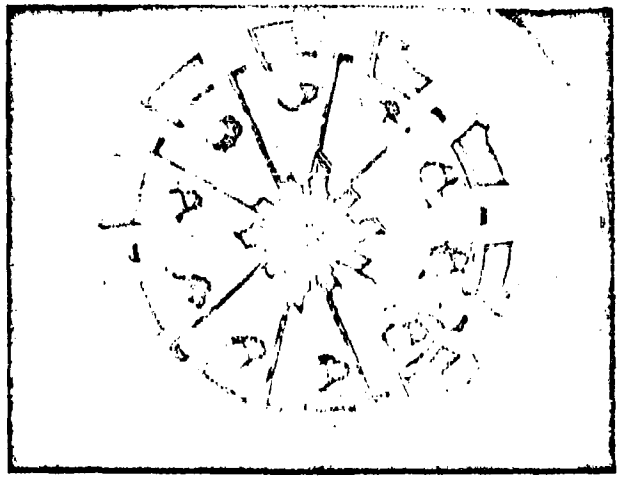


FIGURE 23

Related to metallizing is the placement of a metallic layer upon the back side of the integrated chip or collection of chips upon a wafer, to facilitate the bonding of the chip to a supporting substrate such as a header or ceramic plate.

The current method entails vapor vacuum deposition of gold upon a properly prepared back side of a wafer. After a wafer has been fabricated to completion, the gold is deposited to an estimated layer thickness of about 5000Å, the gold is alloyed to the silicon at approximately the eutectic temperature in an inert and slightly reducing atmosphere. Normally, a bright dendritic film of eutectic material is left upon the wafer surface. However, a few wafers would develop what might be described as a "rusty" surface.

At present, all experiments to control or even directly effect the distribution or occurrence of this phenomena have met with failure. The undesirable features of this "rust" may be illustrated by looking at its properties.

The "rust" appears as a layer of material of unknown composition which remains solid to quite high temperatures, even in the presence of a Au-Si (Liquid) system. As such, it interferes with proper chip to substrate bonding.

As of this writing, alternate systems of backing and die bonding are under consideration and hence, if a solution is not forthcoming, there remains the possibility of circumvention of the problem.

4.4.2 Summary

The metallizing situation may be summed up as follows: The evaporation and etching have been reduced to a routine process. With specific types of circuits some problems have been encountered, these problems have subsequently been resolved. Related to metallizing is the backing of wafers preliminary to "die" bonding to the ceramics or headers. A problem has developed and is now under investigation.

4.5 Testing of Monolithic Integrated Circuits

Five monolithic integrated circuits have reached the testing stage. These are:

1) IF Amplifier
2) NAND/NOR Logic
3) Flip-Flop #1
4) Flip-Flop #2
5) Five Stage Darlington Amplifier

The testing procedure has been broken down into four steps.

1) Check for opens, shorts and voltage breakdowns.
2) Check of tolerance on resistors, h_{FE}, etc.
3) Check low frequency large and small signal parameters.
4) Check high frequency and pulse characteristic.

The transistor curve tracer makes a useful tool for steps one through three.

This testing procedure is coupled with visual examinations and visual defects are correlated with the electrical measurements.

Two circuits with visual defects are shown in Figures 24 and 25. One is a Flip-Flop and the other a NAND/NOR Logic Circuit.

The most interesting test is the use of the "Black Box" approval utilizing the curve tracer as a four terminal network analyzer for "h" parameter measurements.

The results of this work will be reported in subsequent reports.

During the course of this work, a sufficient number of fully integrated circuits has now been constructed to develop several methods of testing the completed units. In this type of development work, a test should show three things:

1) Will the unit perform the intended function.
2) If not, what part of the unit is defective.
3) If possible to determine, what is the physical cause of this electrical defect.

In the fully integrated circuits, as was discussed previously, individual components tend to disappear into the physical structure; thus, it is not always possible or practical to check circuit performance by means of individual components. Two methods have been developed to obtain the required information as discussed above, both of which may be considered as a "black box" type of measurement. The first involves checking the device

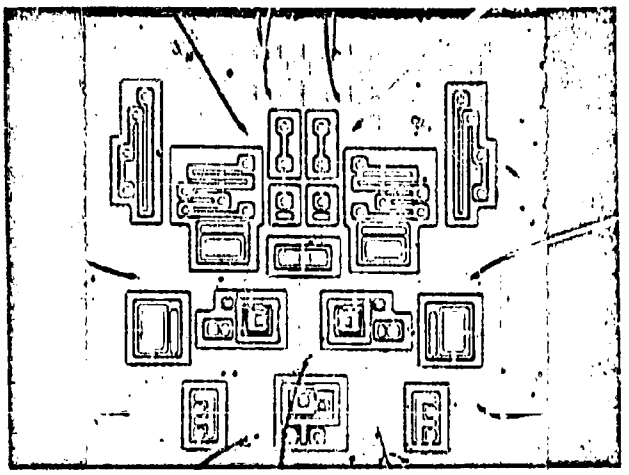


FIGURE 24

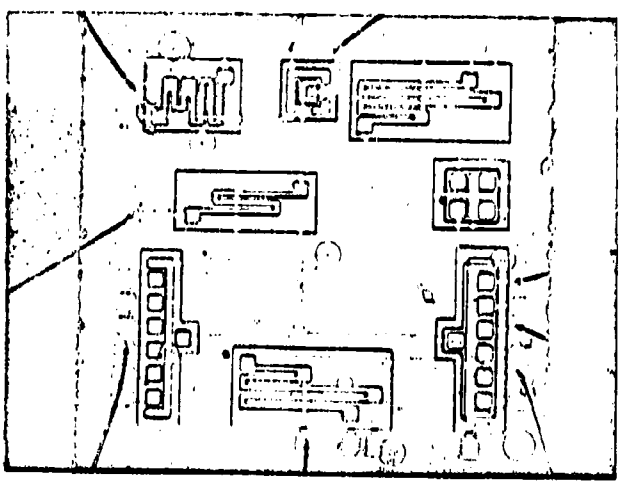


FIGURE 25

characteristics between each of the external connections and the contact to the substrate material. By the proper interpretation of each wave form, it is possible to analyze the performance of the device. The second method consists of applying the operating bias voltages to the circuit and displaying the V_{in} versus V_{out} characteristics on an x-y oscilloscope. This method indicates the actual transfer characteristics, although it is more difficult to analyze failures.

The first method simply consists of a switching arrangement which places the collector and emitter connections of a Tektronix 575 curve tracer between each external contact of the circuit and the circuit substrate. The wave form is obtained for both forward and reverse bias voltages and is compared to those of a working unit. Figure 26 illustrates an example of this type of test on a fully integrated transistor diode logic circuit.

This wave form may be compared to that of a working unit or may be analyzed to determine resistor values, diffusion concentrations and surface effects. In this example, the slope of the trace indicates the resistor value while the break at -6 volts indicates the proper diffusion.

The second method is illustrated in Figure 27. The circuit is connected to all supply and bias voltages required for operation and a sweeping voltage is applied to the input. V_{out} as a function of V_{in} is shown on the Tektronix 536 x-y oscilloscope and the resultant wave form is analyzed or compared to a working unit. Figure 28 and 29 illustrates a typical wave form for the above transistor diode logic circuit. Tests of this

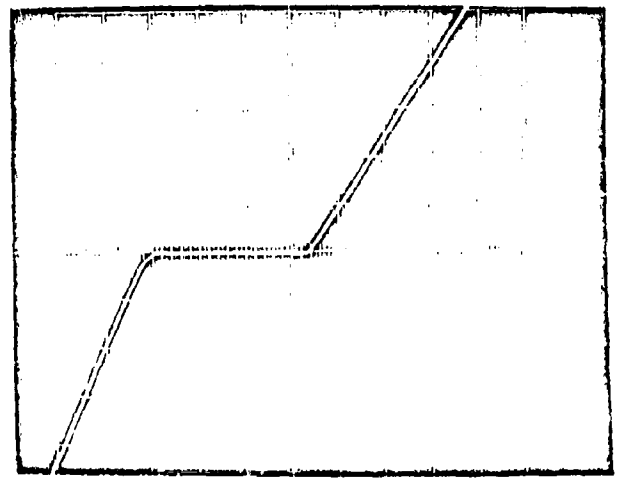


FIGURE 26

Resistor to substrate test wave form of an integrated circuit

Vert: 0.5 Ma/Division

Horz: 2 Volts/Division

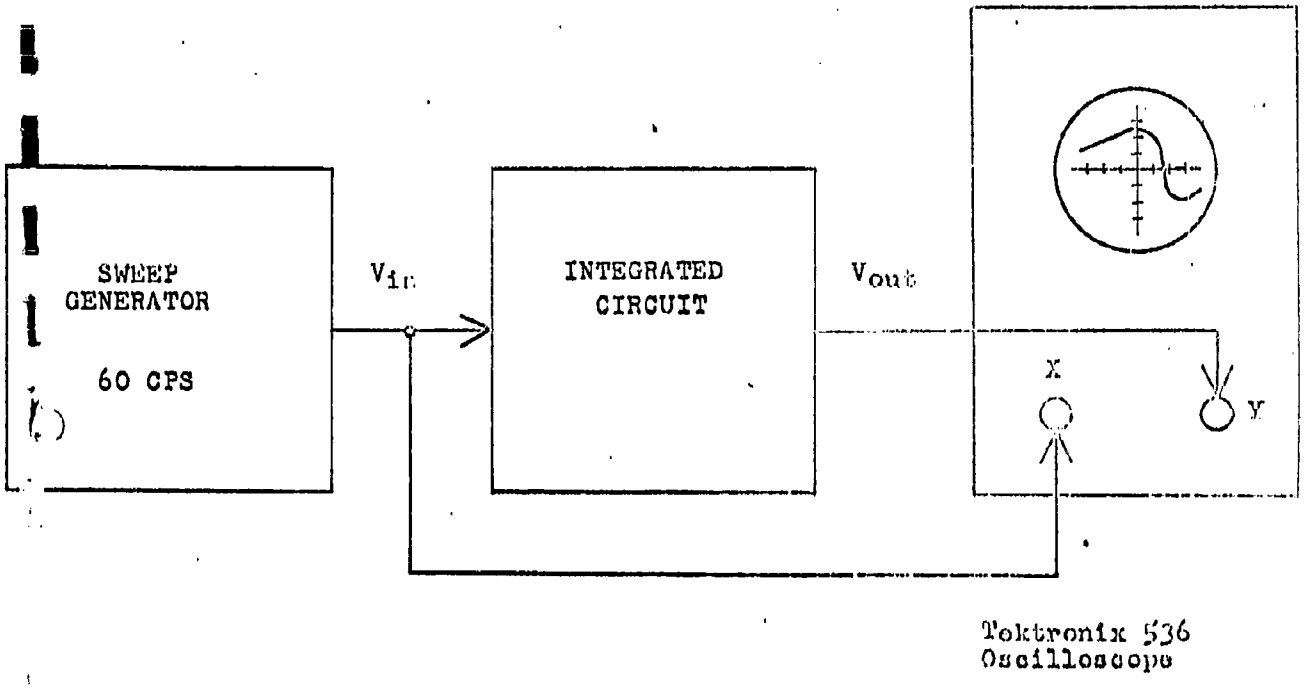


Fig. 27

Transfer Function Test Circuit

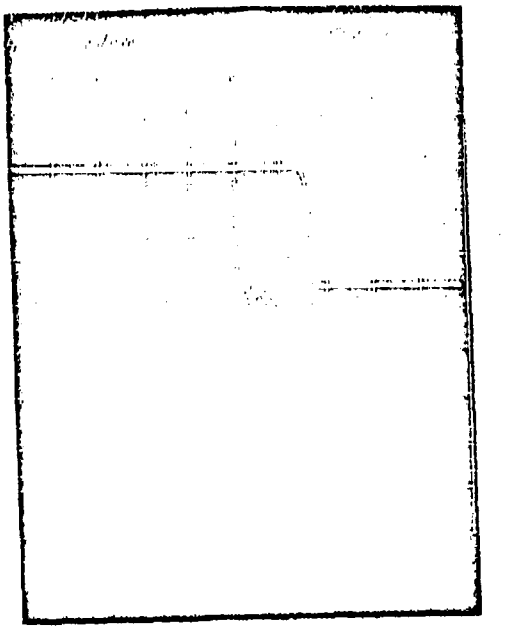


FIGURE 28

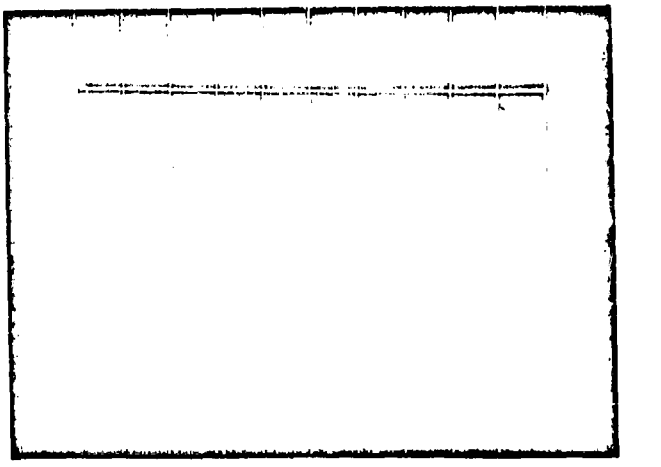


FIGURE 29

nature would be particularly suited for production testing. It should also be noted that performance tests of this type may be applied to any circuit whether linear or digital.

4.6 Optimized Structure for Integrated Circuits

The effort to reduce series collector resistance has proceeded to the base and resistor diffusion operation. Several groups of NAND circuits have been processed through the diffusion and epitaxial growth cycles. The sheet resistance of the collector region after epitaxial growth is sufficiently low to reduce the usefulness of these devices, the resistivity of an undoped epitaxial N-type layer being on the order of .02 ohm cm. The N-type layer is evidently being contaminated by the phosphorus impurities in the N+ layer diffused into the substrate. These phosphorus impurities appear to diffuse into the epitaxial layer very rapidly as it is grown, causing a sharp reduction in the resistivity of the region.

An arsenic diffusion source should eliminate these problems due to out-diffusion of the N-type impurity. The diffusion coefficient for arsenic at the epitaxial growth temperature is 1.6×10^{-13} $cm^2/sec.$ where phosphorus has a diffusion coefficient of 2.8×10^{-12} $cm^2/sec.$ which is an order of magnitude higher. Arsenic has a solubility in silicon in excess of 10^{20} atoms/cc, and will sufficiently "dope" the N+ layer to form a highly conductive path.

4.6.1 High Frequency Integrated Amplifier

A group of high frequency amplifier circuits have been successfully completed and are under evaluation in the transceiver.

This group of amplifier circuits represents the last of this type until a redesign can be performed to make this circuit more compatible with existing processes. Problems in achieving appropriate values for the collector load resistor due to surface channels on the very high resistance substrate and the low collector voltage of these devices make its process undesirable at this time.

4.6.2 MECL Circuits

The MECL gates are being fabricated using the standard four-layer device isolation scheme. Groups of units have been processed through the base diffusion operation. These units are illustrated in Figure 30.

The MECL translator circuits have resistors only in the emitter circuit and a common collector, and may be fabricated as a three-layer device. These units have been processed up to the emitter diffusion operation. They are illustrated in Figure 31.

4.6.3 Transistor Structures in Integrated Circuits

A complete evaluation of the electrical characteristics of the NPN transistor used in integrated circuits has been performed. These units were fabricated on N+N epitaxial silicon in the planar structure. The electrical characteristics of twenty-six of these devices is given in Figure 32. A typical transistor would have the following characteristics:

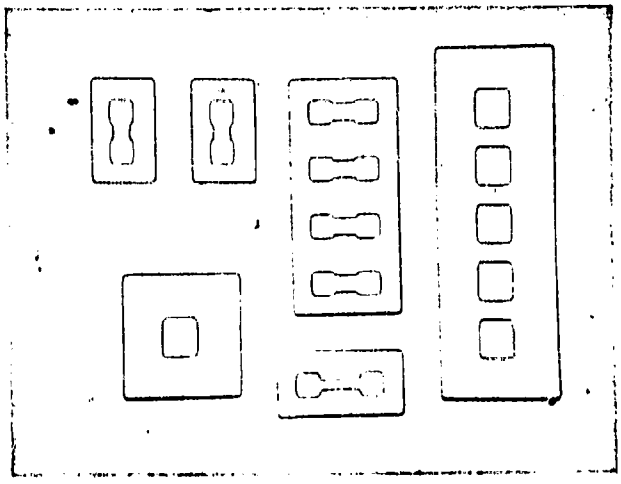


FIGURE 30

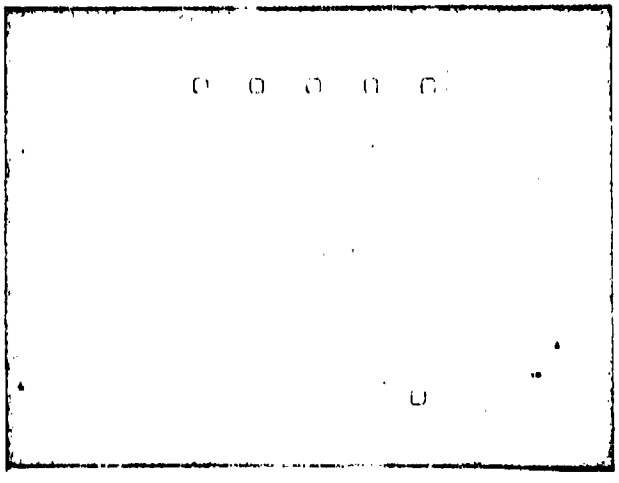


FIGURE 31

DEVICE *INTEGRATED CIRCUITS* LOT Nº *SC-104*

	10μA	10μA	10mA	30V	10V	10mA 1V	10V	0.5V	20V 10mA	20V 10mA	20V 10mA 300MC	20V 10mA 300MC		
UNIT	BV_{cbo}	BV_{ceo}	BV_{eeo}	I_{cbo}	I_{ceo}	h_{FE}	C_{ob}	C_{ib}	f_t	$r_{bb'}C_c$	h_{ie}	h_{fe}	t_{on}	t_{off}
	V	V	V	nA	nA	—	pf	pf	MC	psec	REAL +	IMG −J		
1	52	7.0	30	.28	.13	82	2.70	3.84	545	34	38	27	15	
2	48	7.0	29	1.3	1.0	104	2.76	3.93	670	45	41	40	15	
3	55	7.6	31	2.9	2.5	113	2.41	2.52	880	52	50	52	14	
4	56	7.0	30	.38	.12	116	2.58	2.47	840	49	46	52	14	
5	86	7.4	31	.46	.27	78	2.76	3.43	665	61	56	46	15	
6	66	7.4	33	.52	.82	100	2.46	2.60	645	38	49	38	15	
7	86	6.7	38	.28	.10	36.4	2.49	3.49	415	26	41	16	17	
8	64	7.4	30	.22	.12	104	2.37	2.56	680	38	42	34	15	
9	62	6.4	31	.32	.16	104	2.47	2.42	840	54	48	52	15	
10	82	7.3	34	.58	23	87.8	2.47	2.93	710	46	45	43	16	
11	86	6.8	36	.20	.080	69.5	2.49	2.98	480	29	38	24	17	
12	86	7.2	32	.48	.27	96	2.43	2.71	700	49	50	42	15	
13	75	7.5	33	.62	.32	100	2.35	2.53	740	46	47	44	15	
14	66	7.2	29	.24	.078	108	2.77	2.71	620	40	40	35	15	
15	58	6.4	32	.25	.10	83.2	2.49	2.97	605	34	40	31	16	
16	104	7.3	57	.28	.15	139	2.00	2.21	720	31	48	46	17	
17	108	7.1	53	.22	.11	116	2.15	2.51	670	32	48	36	16	
18	75	7.4	30	.16	.08	125	2.27	2.60	760	—	—	—	—	
19	88	7.2	31	.21	.11	100	2.45	2.70	690	36	43	36	15	
20	75	6.9	34	.32	.11	80.6	2.65	3.03	670	50	44	40	16	
21	88	7.3	33	.38	.16	96	2.45	2.64	640	39	44	36	15	
22	56	6.5	36	.30	.14	44.3	2.51	3.13	420	28	40	18	17	
23	46	6.7	30	.20	.10	104	2.63	2.88	720	48	38	47	17	
24	55	6.8	32	.40	.19	56.6	2.68	3.03	460	27	—	—	—	
25	83	7.6	30	3.6	25	80.6	2.52	3.94	680	53	2	+J 8	15	
26	56	8.0	30	.46	.28	151	2.36	2.34	940	20	51	64	14	
AVE														

NAME *Hal Mayo* DATE *6-28-62*

MAP-016

FIGURE 32

$V_{CE(sat)}$	0.2 Volts
BV_{CBO}	60 Volts
BV_{EBO}	7.0 Volts
BV_{CEO}	30 Volts
I_{CBO}	1.0 Nano Amps
I_{CEO}	0.5 Nano Amps
hFE	80
Cob	2.6 Pico Farads
Cib	3.2 Pico Farads
fT	650 Megacycles
$r_b'C_c$	45 Pico Sec.

The units were not lifetime killed, therefore, no switching data, aside from T_{on}, was taken.

4.7 "Rust" Problem

The "rust" problem is under control and is currently not bothersome. An alternate backing method appears feasible, and simply needs further development to establish itself as acceptable.

Concerning the aging problem of the Al-Au system has related to wire bond strength - it appears that the problem has been circumvented, in that Al wire has now been substituted for the Au wire previously used.

A solderable contacts method has been accomplished upon test patterns. The mechanical technique appears feasible on a laboratory basis. Evaluation using functional circuits is under way and the results will be forthcoming in the near future.

The "rust" problem as outlined in a previous monthly report is troublesome in that it makes die bonding much more difficult. Various experiments, more completely adequate, have been designed in an attempt to isolate the factors necessary to produce the effect. A correlation has been observed and it is upon these results that the present method of deposition is based.

It was observed that those wafers which exhibited "rust" were alloying to the Si substrate during gold deposition. This alloying can be prevented by proper cleaning of the evaporation system, such that radiation to the surface is limited, hence substrate temperatures are held below eutectic temperatures. Alloying during deposition may not be a sufficient condition for rust, but it appears a necessary one. Further studies along this line have been postponed, because of other problems. Many wafers have been processed via the modified gold backing process over the last two months without any evidence of the "rust" problem. It is the observation which supports the idea that alloying is a necessary condition

Some work has been expended upon an alternative backing process. An alternative appears available, and in limited numbers, has provided gratifying results Mechanically, the die bonding is perhaps easier using the newer backing. This backing utilized Ni rather than Au. Thus far, no plagues have appeared. Further work is planned with this process before it will be adopted on a routine basis.

As was mentioned in a previous report, the wire bonding technique was purely an expedient, and that the Au wire to Al strip bond was of a purely transistory nature It has now been

partially worked out. The Al wire can be readily substituted for Au, hence, eliminating the aging problem which occurs in a Al-Au system. Although it appears that the problem is not completely eliminated, since if the header post are Au plated, the problem has only been transferred to another area. This is only partially true. The rate of formation at the inter metallics is reported to be accelerated at a given temperature in the presence of Si, so bonding to a Au plated post is somewhat less hazardous than to a wafer. Secondly, a layer of Au is not essential in wire bonding to the header posts, hence the problem can be eliminated by using other plating schemes on the internal header.

Solderable Contacts:

Mention has been briefly made in prior reports that solderable contacts are feasible. This is indeed the case, in as much as metallized test patterns have been connected in a satisfactory manner to the pins of the 10 pin TO-5 header Joining to the metal test pattern and again to the pins is accomplished by a high temperature soldering or brazing operation, thus producing what appears to be a satisfactory mechanical and electrical connection.

Feasibility has been demonstrated only at a laboratory level. Samples fabricated to-date have not utilized any jigging facilities. These will be inherent in the process, however, that the assembly will be self jigging to a great extent. This is evident upon inspection of the "pin wheel" contacting plate which is currently being used at this phase of the development.

4.8 Process Control

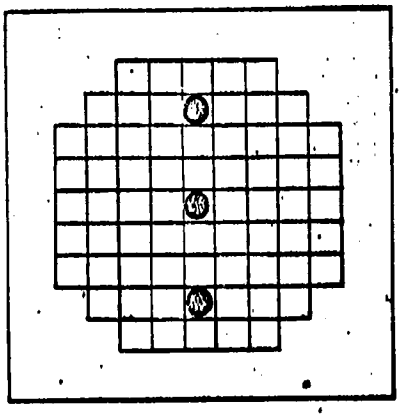
One of the basic problems in the production of integrated circuits is the ability to successfully monitor the processes involved and thereby achieve a high degree of quality control. This problem is compounded by the fact that in integrated circuitry there are many different circuits involved and hence a standardized quality control process becomes difficult. Since the basic sequence of processes involved in the fabrication of any integrated circuit is somewhat the same, however, it becomes feasible to devise a single control system which will function for all of the various integrated circuits being designed and produced.

During this report period such a single control system for use with all integrated circuits has been designed, and, as a test pattern, is being incorporated in the integrated circuit process.

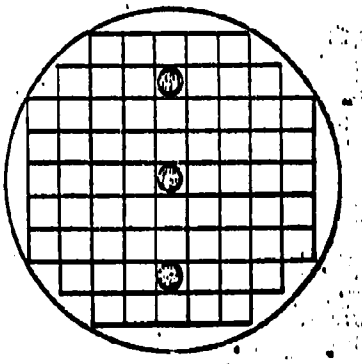
4.8.1 Test Patterns

The test patterns are used for the measurement of transistor parameters, the quality of diffused junctions, resistivity, alignment, resolution and many other measurements needed for the close control of the integrated circuit process.

Thepattern is an integral part of the photoresist mask and is positioned in the mask grid as shown in Figure 33. Using the photoresist masks, the test pattern is formed on the wafer by successive oxidation steps. As an example of the test pattern



Test Patterns in Photoresist Mask
Figure 33



Test Patterns on Wafer
Figure 34

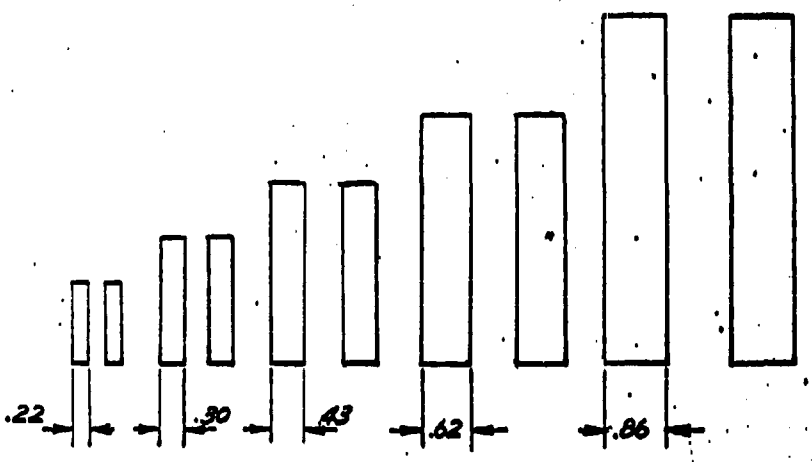
concept, Figure 35 and 36 is an illustration of monitoring the resolution of the photolithographic process. This control pattern concept has been very valuable in measuring each diffusion and masking step in the integrated circuit process.

4.9 Resistor Evaluation in Integrated Circuits

The universal logic circuit of the type 705 has been completed by using passivated-planar-epitaxial techniques. Functional characteristics are now being evaluated. This section is a report on the resistor evaluations so far completed.

Figure 37 shows the locations of the points evaluated on a 100 mil square die bonded to a TO-5 header. These points were arbitrarily selected for evaluation; and the numbers in the figure refer to the standard pin numbers of the header. The resistors were formed in the circuit by P-type impurities being diffused into an N-type isolation region on a P-type substrate. A three dimensional sketch is shown in Figure 38.

The results of the evaluations for three circuits are listed in Figure 39. The range of the percentage difference between the design values and the tested values varied from 40% to 208% with a mean of 102%. A thorough check of the design, process monitoring tests, and operations control is being conducted. Improvements will be reported later. The normalized variance with each circuit is plotted in Figure 40 for every resistor tested. It appears that the 0.4K, 0.8K and 3.8K resistances have a definite relation to the designed value, indicating in all probability, the process control was constant. However, the 5.0K resistors have random values which implies the



Layout of Resolution Patterns

Figure 35

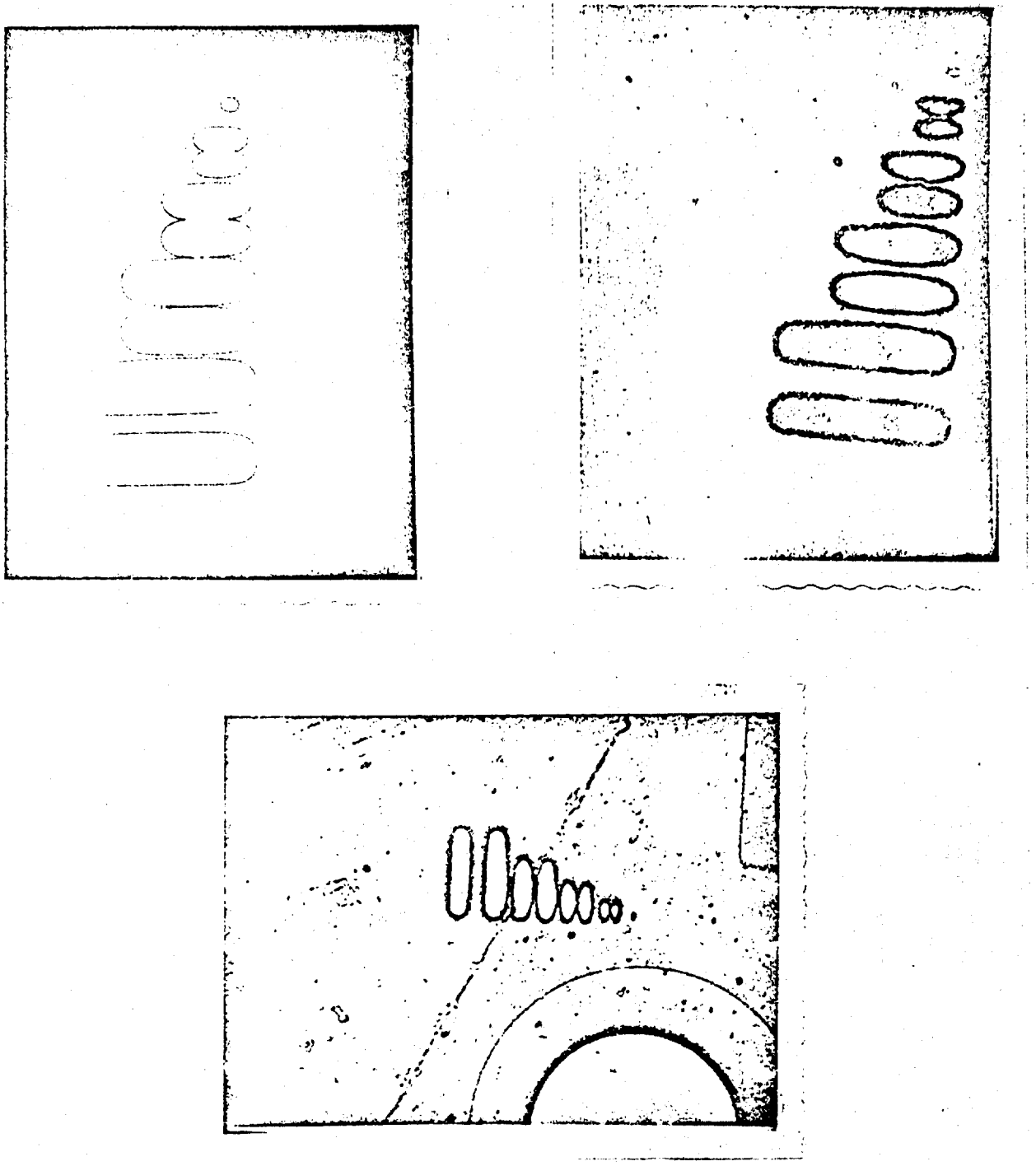


FIGURE 36
Resolution Test Patterns

design control was not carried over to the high value resistances.

Temperature stability studies were investigated and the results are displayed in Figures 41, 42, 43 and 44. The temperature coefficient of resistance appears to approach zero in the neighborhood of 220 K (-53°C). At lower temperatures the temperature coefficient of resistance is negative; and at higher temperatures a positive temperature coefficient exists. This behavior is characteristic of the doping level of the semiconductors employed in the resistors measured. The thermal coefficient of resistance was computed for each circuit from the slope of the curve at 55°C. The values obtained from Figures 41 to 43 inclusive are shown below in Figure 45. Essentially, circuits B and C have identical temperature coefficients.

Figure 45
Some Thermal Coefficients of Resistance

	Coefficient of Resistance at 55°C
Circuit A	4410 ppm/°C
Circuit B	2060
Circuit C	2050
Average	2840 ppm/°C

This similarity agrees with that obtained in Figure 40 and again indicates the consistency of the design to control the resistances measured. Figure 44 compares the measured resistances against the designed values. The two curves are in agreement below 60 C (140°F).

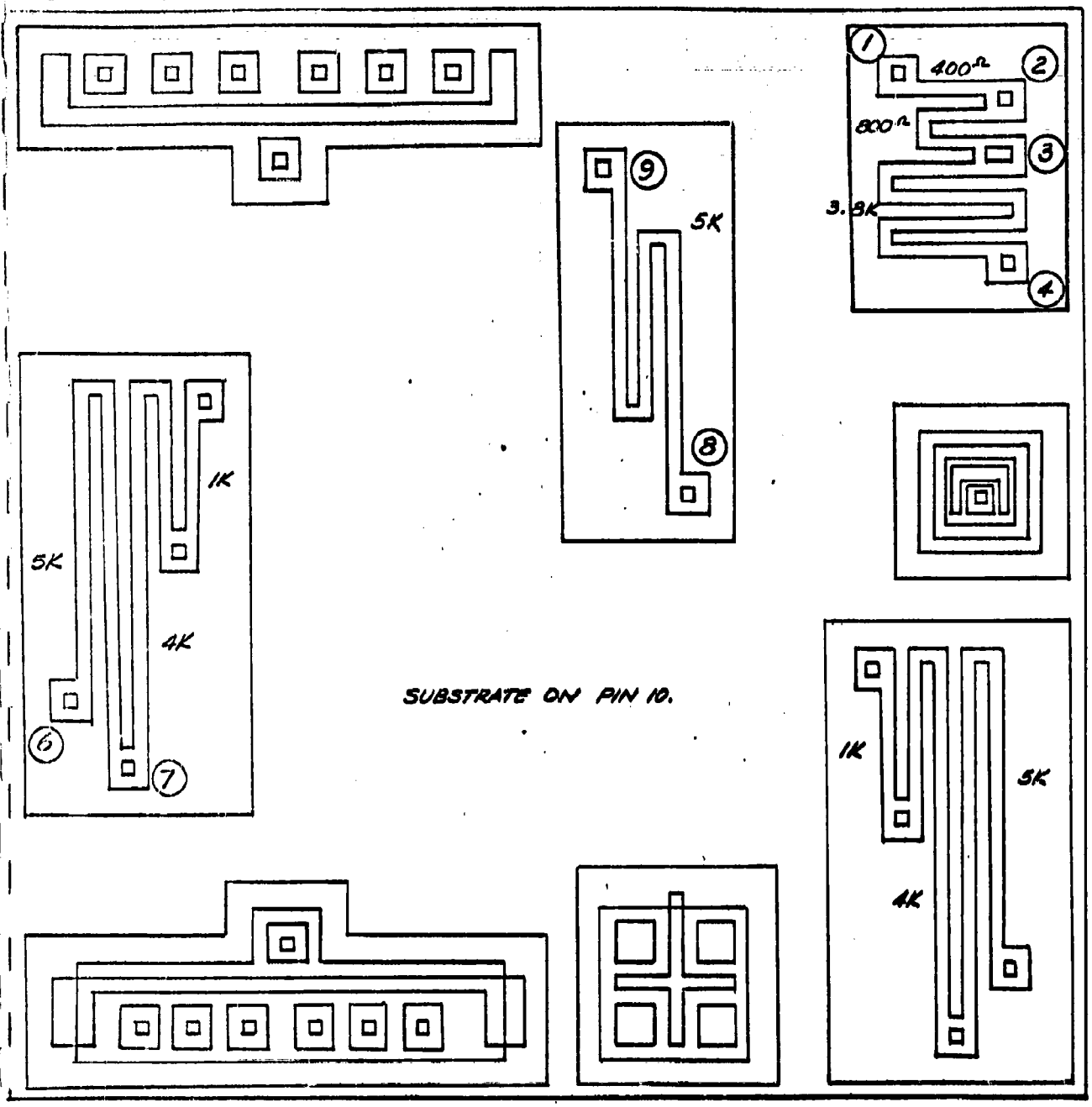


Figure 37

Type 705 Universal Logic Circuit
as Bonded for Resistor Evaluation

Figure 38

A Typical P-type Resistor Used in Integrated Circuits

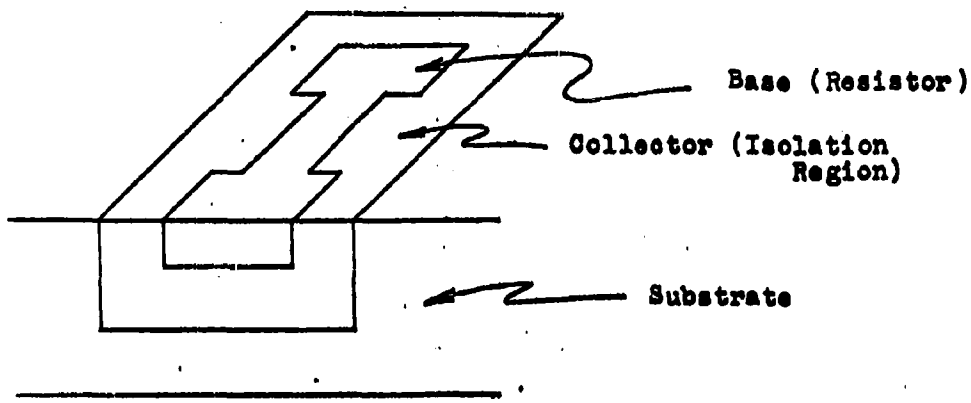


FIGURE 39

Resistor Values of an Evaluated Integrated Circuit

Resistor	Circuit	Desired Value	Measured Value	Per Cent Error	Normalized Value
1 - 2	A	400 Ω	800 Ω	100%	200 Ω
	B	400 Ω	1230 Ω	208%	308 Ω
	C	400 Ω	1230 Ω	208%	308 Ω
	Average	400 Ω	1087 Ω	172%	272 Ω
2 - 3	A	800 Ω	1090 Ω	36%	136 Ω
	B	800 Ω	1670 Ω	109%	209 Ω
	C	800 Ω	1770 Ω	121%	221 Ω
	Average	800 Ω	1510 Ω	89%	189 Ω
3 - 4	A	3800 Ω	4720 Ω	24%	124 Ω
	B	3800 Ω	7440 Ω	96%	196 Ω
	C	3800 Ω	7350 Ω	93%	193 Ω
	Average	3800 Ω	6503 Ω	71%	171 Ω
6 - 7	A	5000 Ω	7970 Ω	59%	159 Ω
	B	5000 Ω	11110 Ω	50%	150 Ω
	C	5000 Ω	9460 Ω	122%	222 Ω
8 - 9	A	5000 Ω	7520 Ω	40%	140 Ω
	B	5000 Ω	7000 Ω	89%	189 Ω
	C	5000 Ω	10320 Ω	106%	206 Ω
	Average	5000 Ω	8897 Ω	78%	178 Ω

Figure 40

Resistances Normalized with Respect to Design Objective Values for the Circuits Evaluated

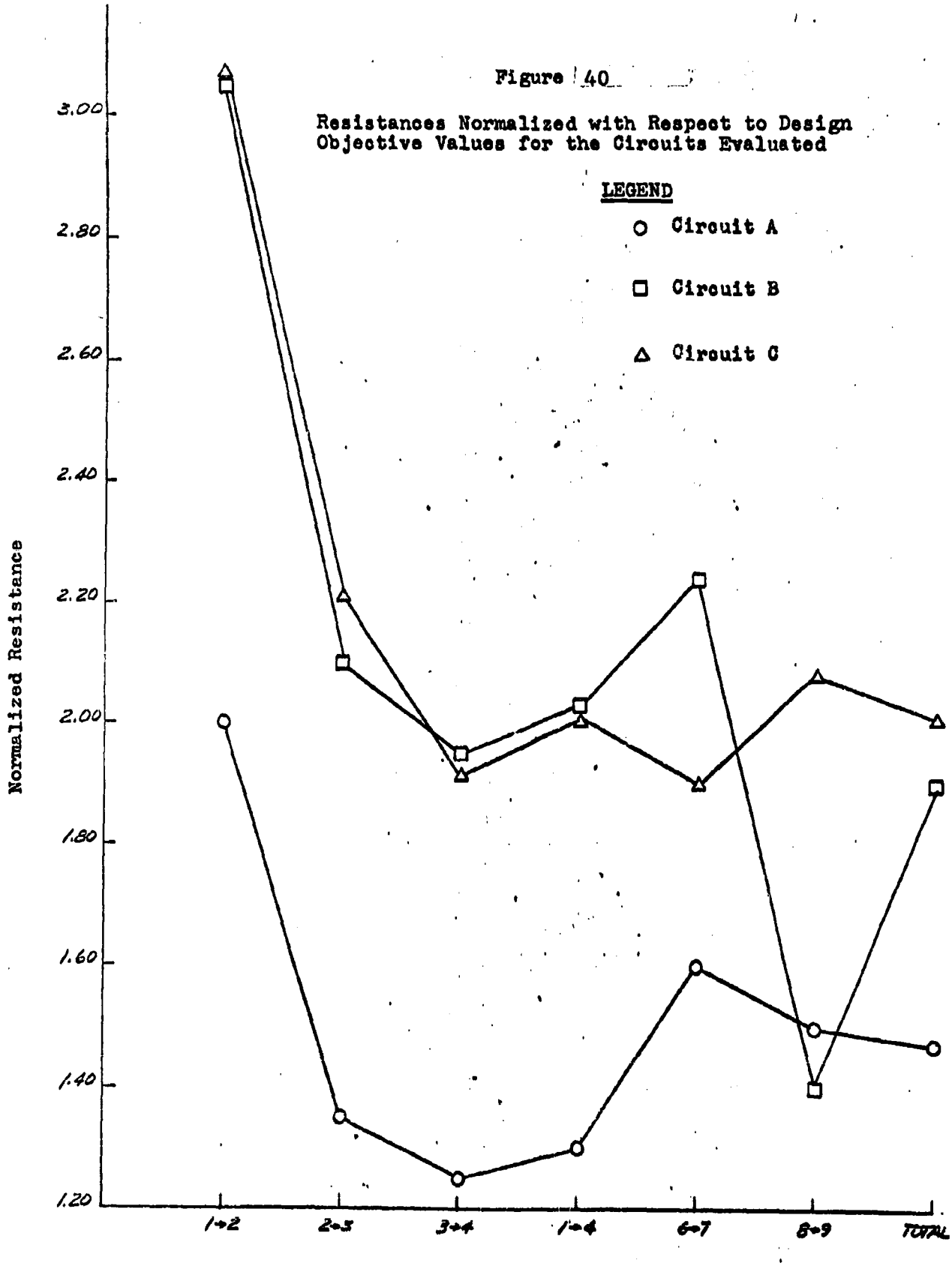


Figure 41

Average Temperature Coefficients
for Resistors in Circuit A

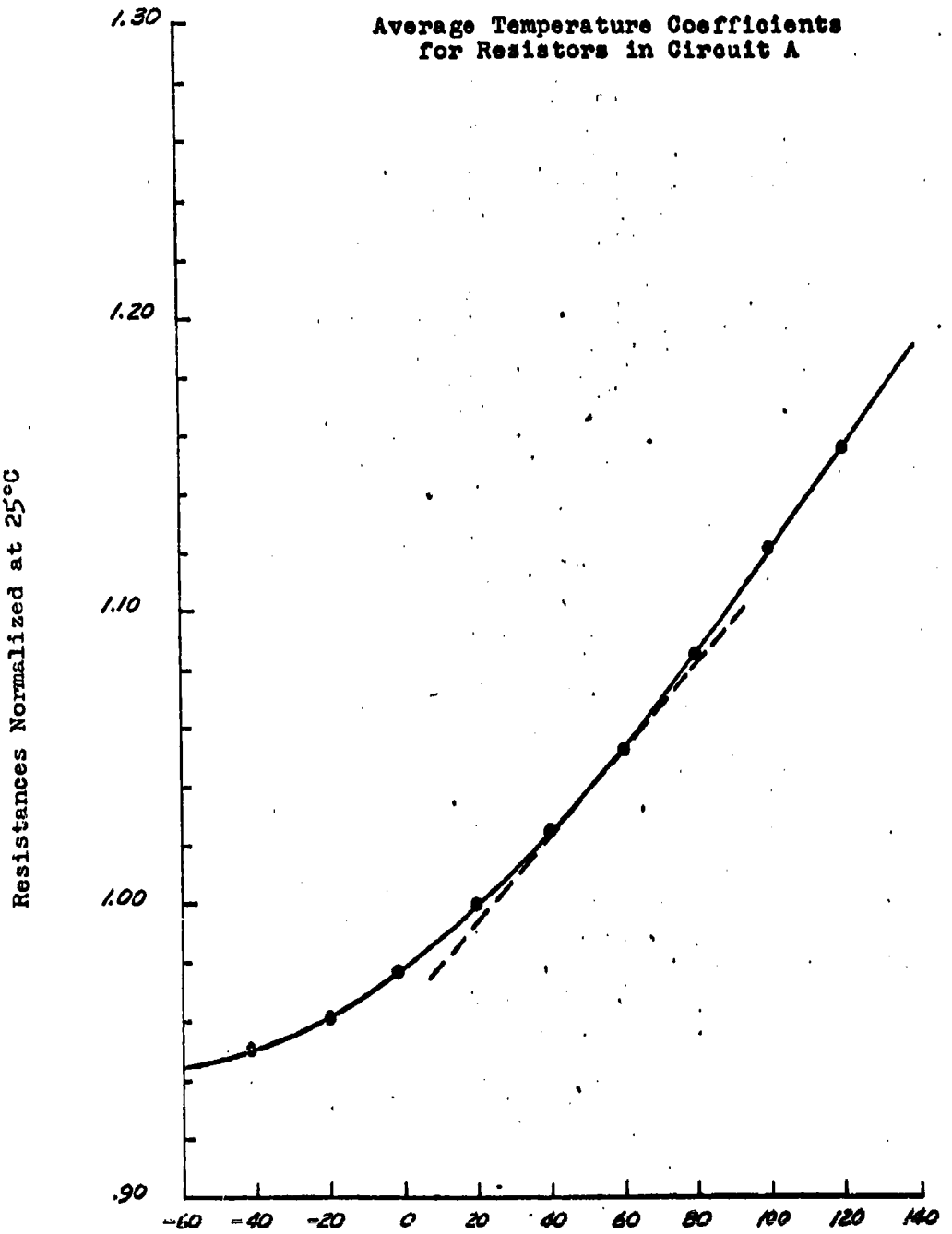


Figure 42

Average Temperature Coefficients for Resistors in Circuit B

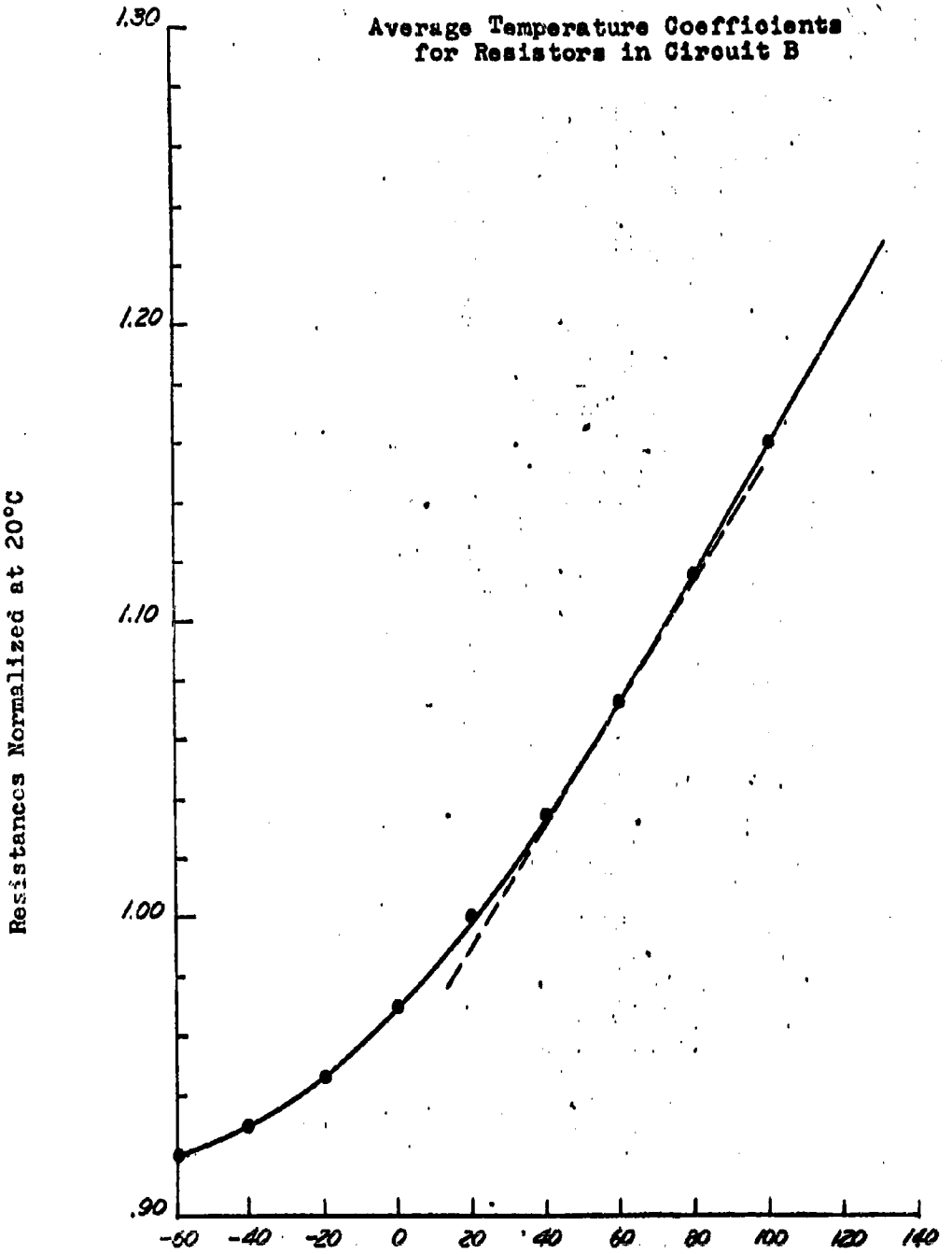


Figure 43

Average Temperature Coefficients
for Resistors in Circuit C

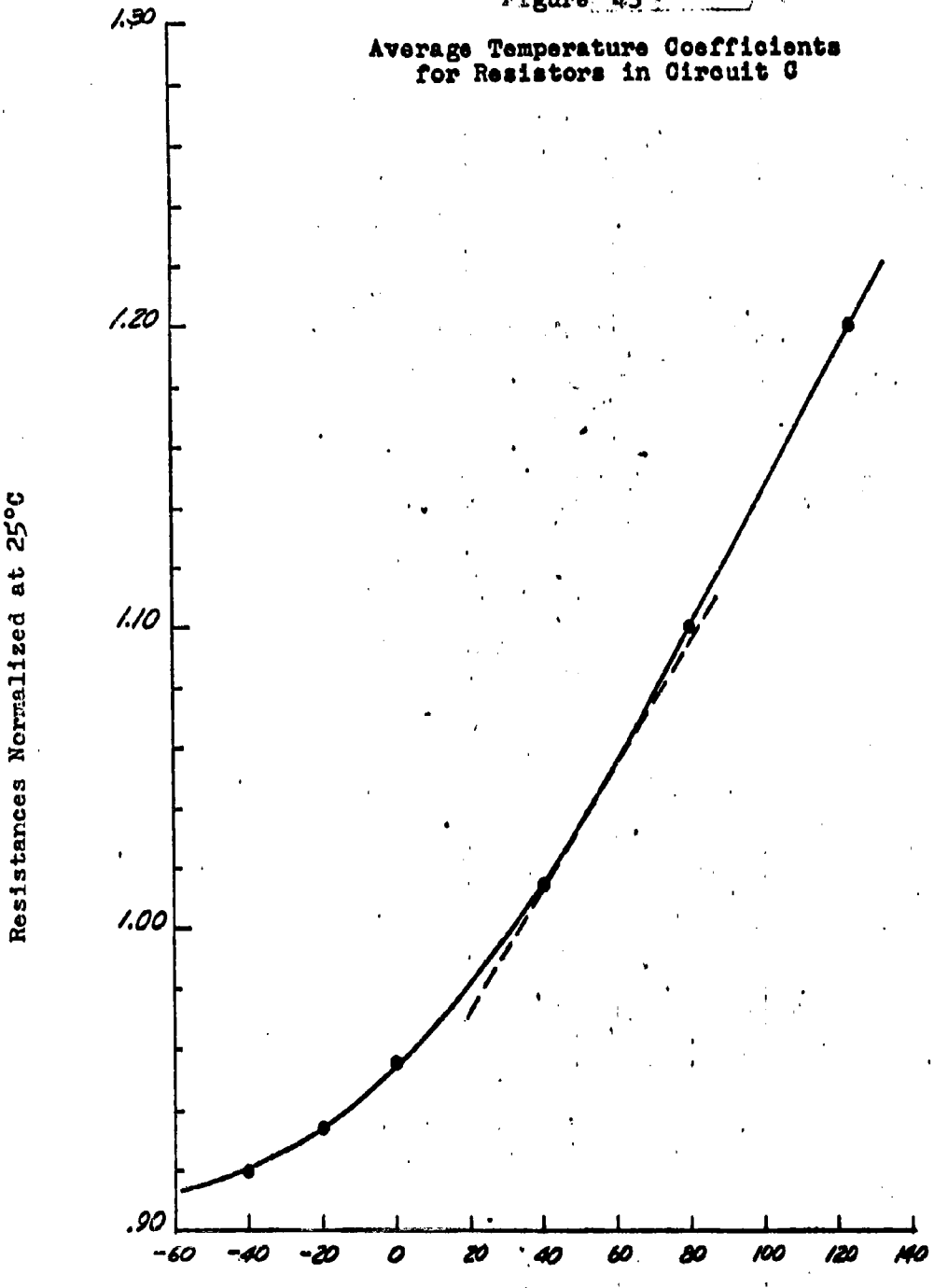
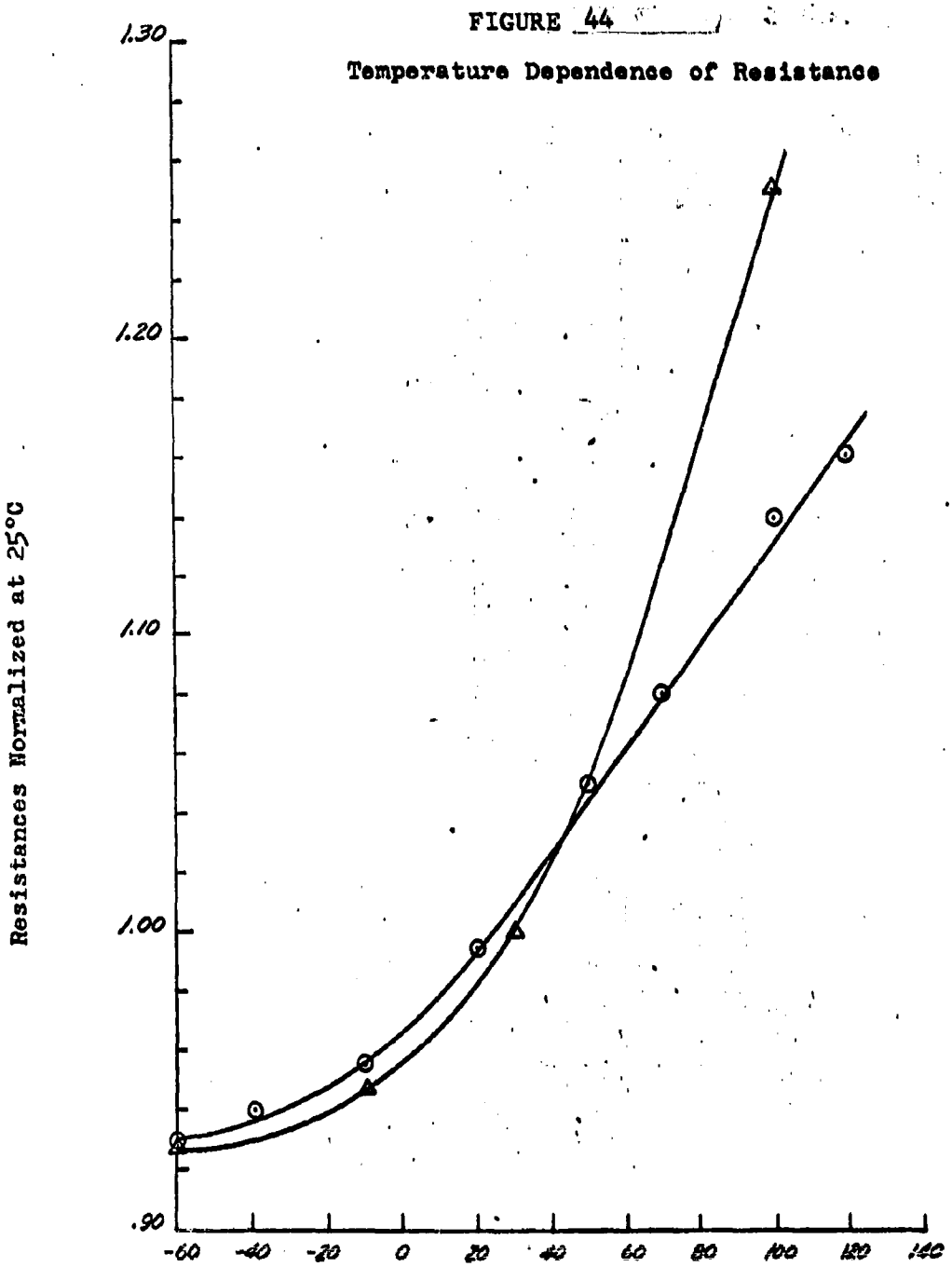


FIGURE 44

Temperature Dependence of Resistance



LEGEND

⊙ Resistance Calculated from the Doping Impurity Concentrations Used.

△ Average Normalized Resistance Measured in the Three Circuits.

5.0 ADVANCED CIRCUIT DESIGN STUDIES

5.1 DCTL (Direct Coupled Transistor Logic)

The 8-bit arithmetic unit and its associated printed circuit cards are now completed. Since the printed cards were grounded to the rack at only one point on each card, considerable pulse degradation due to ground loops was observed. This problem was solved by installation of a more complete ground bus system and clip arrangement to ground the opposite edge of each card.

The unit was checked for accurate logical operation. Then data was taken to determine average delay across each type logic block. A V_{cc} of 5 v applies to the data given here, but delays varied only a few percent with V_{cc} = 3 to 7 volts.

3- or 8-input "OR" Gate - Av. Delay = 26 nsec.
3-input "AND" Gate - Av. Delay = 34 nsec.
7-input "AND" Gate - Av. Delay = 40 nsec.
Half-Adder - Av. Delay = 20 nsec.

It was observed that the lower half-adder of a given full-adder had much more delay (≈20 nsec more) than the upper half-adder. This was due to the degradation of the output pulse of the single inverter being used to drive the $\overline{X}$ inputs of all 8 lower half-adders. The large fan-out at this node resulted in such trailing edge delay as to give the lower half-adder the appearance of being much slower. To eliminate this effect it would be necessary to drive each bit's $\overline{X}$ input from a separate inverter.

Tests were made to determine carry propagation delays of the total system in both parallel-parallel and ripple-carry modes. These tests were made as follows: The Y, $\overline{Y}$ inputs were made static DC. The X, $\overline{X}$ inputs were pulsed with an E-H Research Labs Model 131 generator. The inputs to bit 1 were X + 1 (pulsed), Y = 1. All 7 other bit inputs were made X = 1, Y = 0. Thus, a carry was generated in bit 1 and propagated to the bit 8 carry output.

Data given is only for leading edge delay. Because of the test set up described, the trailing edge of the bit 8 carry output was triggered by the X-input pulse's trailing edge being propagated only through the bit 8 full-adder. Therefore, the trailing edge is of no significance in determining delays of the total system. This is the case in both ripple and parallel-parallel operation.

Propagation Path = e_{in} to eighth bit carry output

MODE	V_{cc}	Leading Edge Delay
Par.-Par.	3v	77 nsec
Ripple	3v	204 nsec
Par.-Par.	5v	70 nsec
Ripple	5v	191 nsec
Par.-Par.	7v	72 nsec
Ripple	7v	203 nsec

A detailed observation of slivers was made. These slivers usually take the form of short spikes in the sum or carry outputs of higher-order bits when these outputs should logically be zero. They can be identified as occurring at times when the output pulse would be rising or falling if an output pulse were present.

Slivers of this type were found to arise from two effects:

1) Unequal delays on inputs to "AND" gates, resulting in short "time gaps" in the switching period during which no input is as high as the threshold voltage of the input transistors. This effect is observable, although not so great, even if all inputs are "in phase" since even then one input may fall below V_T before another input rises to V_T.

2) Unequal delays on inputs to half-adder. This is the inevitable result of the fact that some inputs must pass through more logic blocks than others.

Another effect which might be termed a "DC sliver", is seen in the half-adder sum and carry outputs if the DC X, $\overline{X}$ is slowly varied while Y, $\overline{Y}$ is held static. There is a very narrow range of e_{in} for which a sum output will be produced. Assuming all devices in the half-adder are identical in other respects, this range of e_{in} is a function of the difference between the threshold voltage of the device fed directly by X and the threshold voltage of the inverter which drives the $\overline{X}$ input.

During the next period, the entire 8-bit arithmetic unit will be tested at high and low temperatures, and results compared with those obtained at room temperature.

5.1.1 DCTL Current Hogging Analysis

The dependence of DCTL design on device parameters has been partially investigated. The parametric equations derived by

Ebers and Moll were used to determine the variation of circuit voltages with a variation of device parameters.

The number of transistor bases that may be connected to any given voltage node (fan out) is greatly curtailed by the variation of the different transistor input characteristics.

$$V_{BES} = r_b' I_b + O_{BES} + (I_c + I_b)\, r_E \qquad (1)$$

r_b' = base body resistance
r_E = emitter body resistance
O_{BES} = base to emitter junction potential

$$V_{BES}' = V_{BES} \quad (I_c + I_b)\, r_E' = r_b I_b + O_{BES} \qquad (2)$$

$$O_{BES} = \frac{KT}{q} \ln \left[\frac{I_b + (1 - \alpha_I)\, I_c}{I_{EO}} \right] \qquad (3)$$

α_I = inverse alpha
I_{EO} = base-emitter leakage current

The change in the input characteristics from device to device can be examined by setting I_c and I_b at a constant value in equation (2). Here we have:

$$V_{BES}' = r_b' K_1 + \frac{KT}{q} \ln \frac{K_1}{I_{eo}} + \frac{KT}{q} \ln (1 + (1 - \alpha_I)\, K_2)$$

The controlling parameters in this case are I_{EO}; r_b' and αI.

To make the device parameters least effective in varying the input characteristics, the addition of an external resistor in series with the base is necessary.

The input characteristic on collector current can be determined by defining a change in base-emitter voltage as a function of the change in collector current.

$$\frac{[V_{BES}]}{[I_c]} = \frac{KT}{q} \frac{I_{eo}}{I_{eo}} \frac{(1-\alpha_I)}{I_b + (1-\alpha_I) I_c}$$

$$\lim_{\alpha_I \to 0} \frac{V_{BES}}{I_c} = \frac{KT}{q} \frac{1}{I_b + I_c}$$

$$\lim_{\alpha_1 \to 1} \frac{V_{BES}}{I_c} = \frac{1-\alpha_I}{I_b}$$

$$\int_{V_{BE_1}}^{V_{BE_2}} dV_{BES} = \int_{I_{c_1}}^{I_{c_2}} \frac{KT}{q} \frac{(1-\alpha_I)}{I_b + (1-\alpha_I) I_b} dI_c$$

$$\Delta V_{BES} = \frac{KT}{q} \ln \frac{I_b + (1-\alpha_I) I_{c_2}}{I_b + (1-\alpha_I) I_{c_1}}$$

From the above we see that in the limit of high α_1, we have little dependence of the input characteristic on collector current. This is indeed the case, and high values of inverse alpha are beneficial <u>if</u> the value of alpha can be closely controlled.

5.2 MECL

The piece-wise linear analysis technique was used for the steady-state design of the basic MECL logic block.

Several multiple chip MECL circuits have been received. Preliminary data indicates no observable degradation between the breadboard circuit and the multiple chip circuit. The printed card layout for the 10-bit MECL adder is about 50% complete. Layout of MECL is somewhat more difficult than the DCTL layout due to the number of power supplies. The multiple chip circuits are being used since they should be a closer similation of the integrated circuit than the printed circuit type used in DCTL.

The arithmetic adder should provide a good comparison of DCTL, MECL and DTL under dynamic operating conditions.

5.3 DTL

During the quarter, work on DTL has continued, with emphasis placed on measurement of switching times for various power levels, impedance levels and configurations.

Figure 1 shows switching time vs. power level measured for three of the most important possible configurations obtainable in DTL. The data was obtained by varying impedance level in a chain of DTL devices built up in discrete form as shown in Figure 1. This chain represents the "ideal" case in the sense that each module sees only a fan-out of 1.

Figure 2 shows a similar curve obtained with 10pf capacitors added as shown to simulate fan-in and fan-out line loads.

A "research vehicle" DTL circuit was designed and submitted for device fabrication. Figure 3 shows the predicted

"worst case" fan-out vs. power supply voltage and tolerance for typical environmental conditions. Figure 4 shows measured average propagation times for this circuit vs. power supply voltages obtained using discrete models of this circuit. Heavy fan-out loading was simulated by adding 150 pf capacitors from output collectors to ground to the circuits shown in Figure 3.

An interesting comparison between DTL, MECL and DCTL is shown in Figure 5 where average propagation times vs. power level measurements for nominal models of the three logic schemes have been consolidated. The data shown plotted in Figure 5 was not all taken in the same manner - impedance levels having been changed for the DTL and MECL curves and power supply levels for DCTL.

Analytical work on DTL continued with emphasis being placed on the design of an optimum wafer which could be used with different metallization patterns to obtain leading edge triggered flip-flops, trailing edge triggered flip-flops, and numerous "NAND"-"NOR" logic gate types.

Figures 6 to 10 show the results of DC Worst Case Analysis and propagation time measurements made for two discrete versions of research vehicle NAND circuits that are under consideration. Note that diodes have replaced the multiple emitter input transistors used previously. This design change was instituted when measurements of the multiple emitter design under similated fan out conditions revealed that the inverse beta of transistors in the fan out stages was causing excessive loading of the driving stage. In fact, it was discovered that even though the inverse beta was very low (less than .5) in the 2N834 devices used, a fan out of one was sufficient to keep the collector of the high

impedance design from returning fully to V_{cc} when the output device shut off.

Design work on the DTL optimum wafer has produced an interesting possibility. Figures 11 through 14 show how one DTL assembly could be used for five different circuits by merely changing external connections. Two types of flip-flops can be made by cross coupling two of the DTL devices as shown in Figures 11 and 12. The five input "NAND" junction can be obtained using one device as shown in Figure 13. The multiple diode assembly as shown in Figure 10 could be used to increase the fan in of the five input "NAND" of Figure 13.

An alternate way of obtaining the functions desirable above is also being investigated. This technique will use a dual "NAND" in each device and use different metallization masks to get the desired interconnections.

The leading edge and trailing edge triggered flip-flop designs as shown in Figures 11 and 12 were tested extensively in discrete form. Switching performance was found similar to the DTL "NAND" gates, with total transition times equivalent to the propagation time for two stages of "NAND" gates. Repetition rates of up to 10 mc were observed for the toggle or "T" flip-flop design.

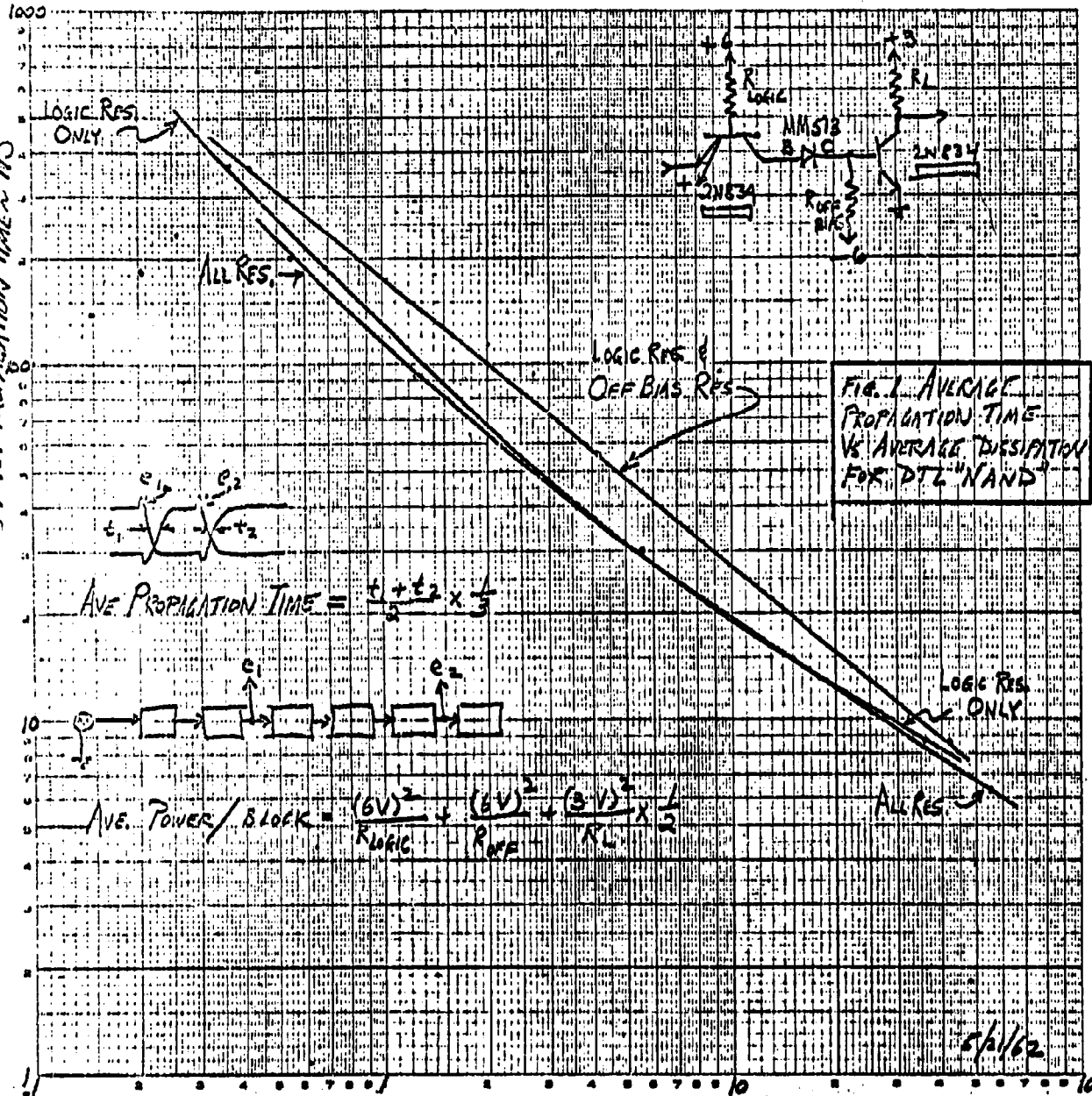


FIG. 1 AVERAGE PROPAGATION TIME VS AVERAGE DISSIPATION FOR DTL "NAND"

AVE. POWER PER LOGIC BLOCK ~ MILLIWATTS

FIGURE 1

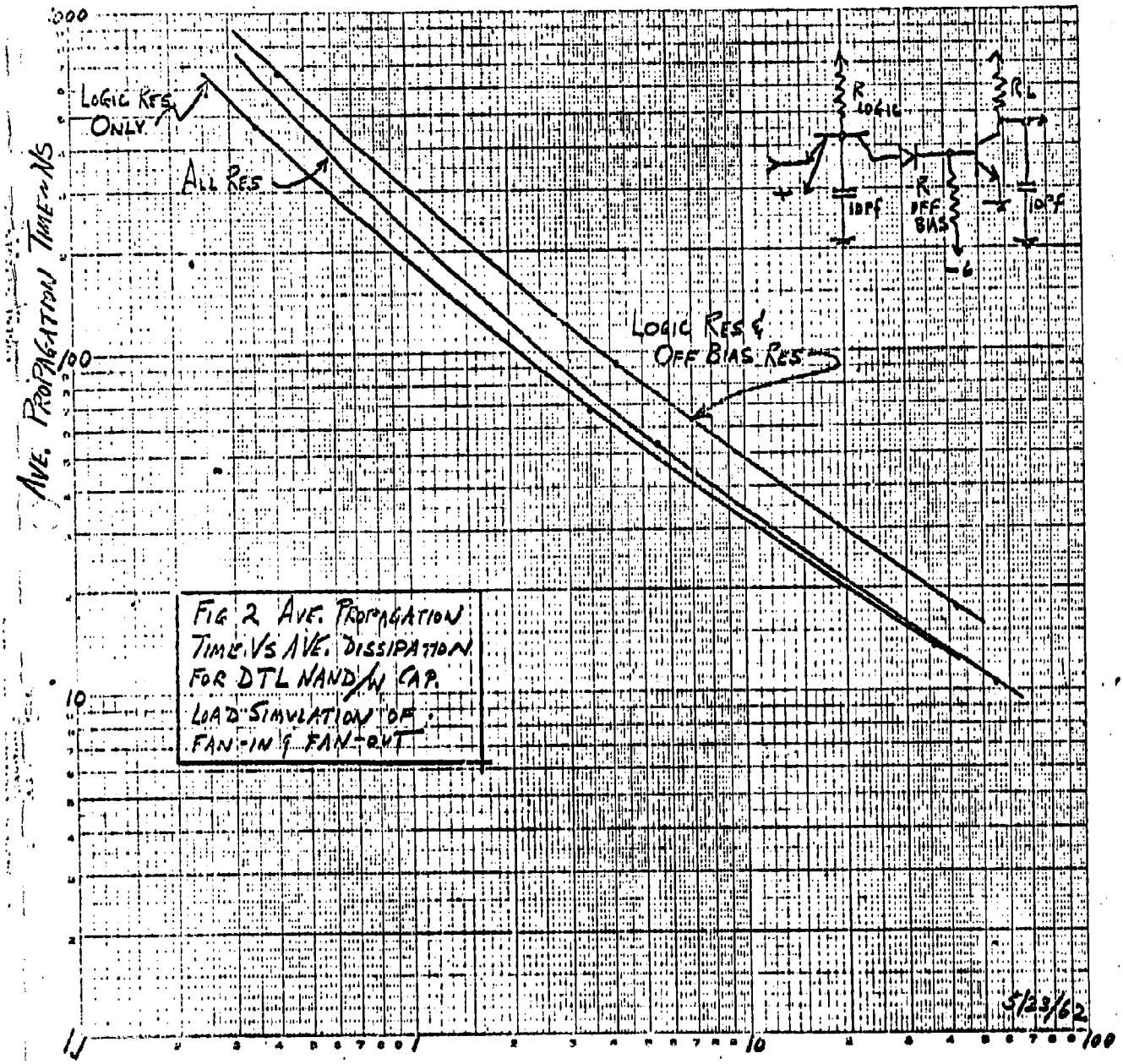

AVE. PROPAGATION TIME-NS
LOGIC RES ONLY
ALL RES
LOGIC RES & OFF BIAS RES
R LOGIC
R OFF BIAS
-6
10pf
10pf
RL
FIG 2 AVE. PROPAGATION TIME VS AVE. DISSIPATION FOR DTL NAND/NOR CAP. LOAD SIMULATION OF FAN-IN & FAN-OUT
5/23/62
AVE. POWER PER LOGIC BLOCK IN MILLIWATTS

FIGURE 2

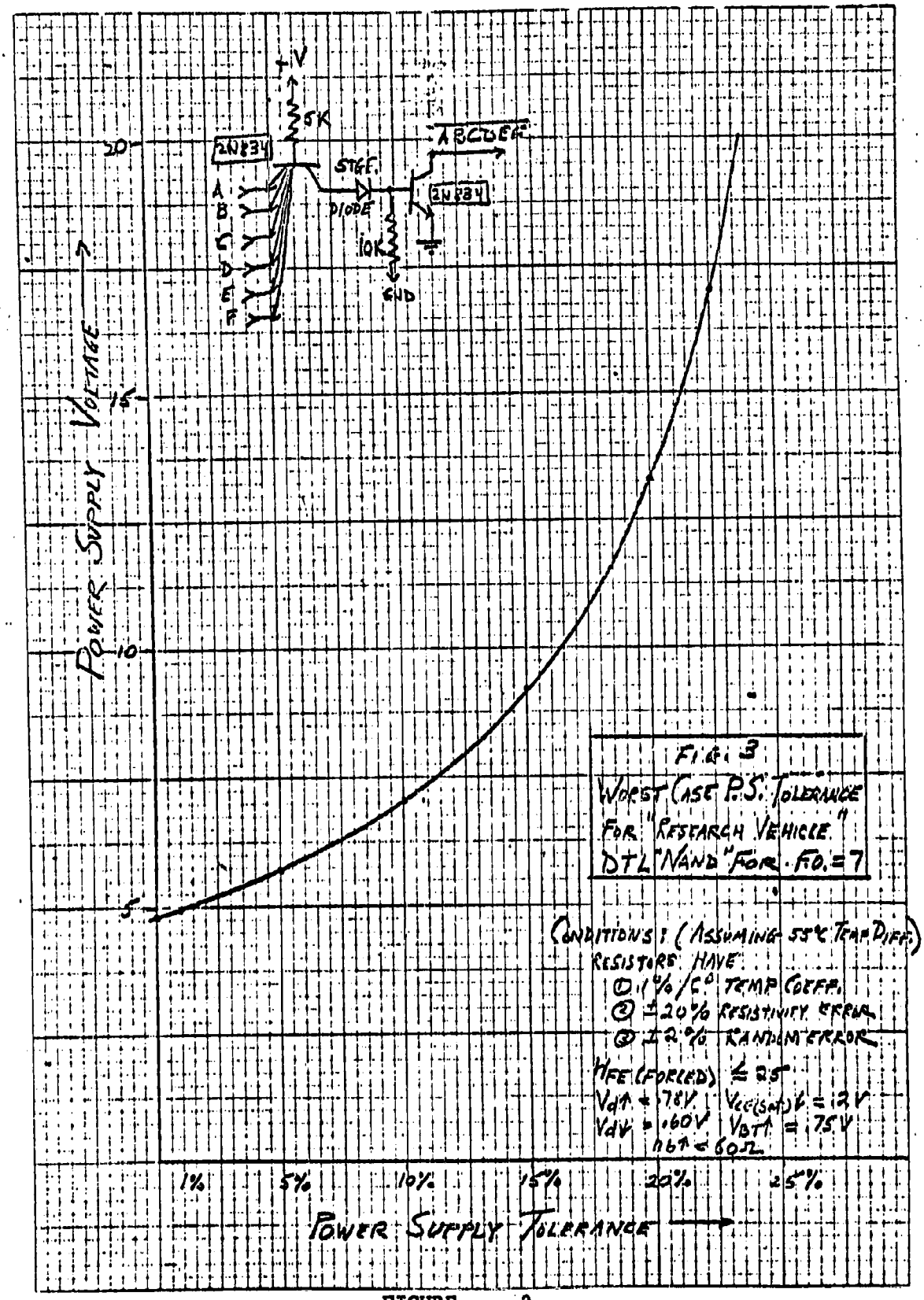

+V
5K
2N834
A
B
C
D
E
F
STGF.
DIODE
10K
GND
ABCDEF
2N834
20
15
10
5
POWER SUPPLY VOLTAGE
1%
5%
10%
15%
20%
25%
POWER SUPPLY TOLERANCE
FIG. 3
WORST CASE P.S. TOLERANCE
FOR "RESEARCH VEHICLE"
DTL "NAND" FOR FO.=7
CONDITIONS: (ASSUMING 55°C TEMP DIFF.)
RESISTORS HAVE
① .1%/C° TEMP COEFF.
② ±20% RESISTIVITY ERROR
③ ±2% RANDOM ERROR
HFE (FORCED) ≥ 25
VdT = .78V. VCE(SAT) V = .2V
VdV = .60V VBT = .75V
rbT = 60Ω

FIGURE 3

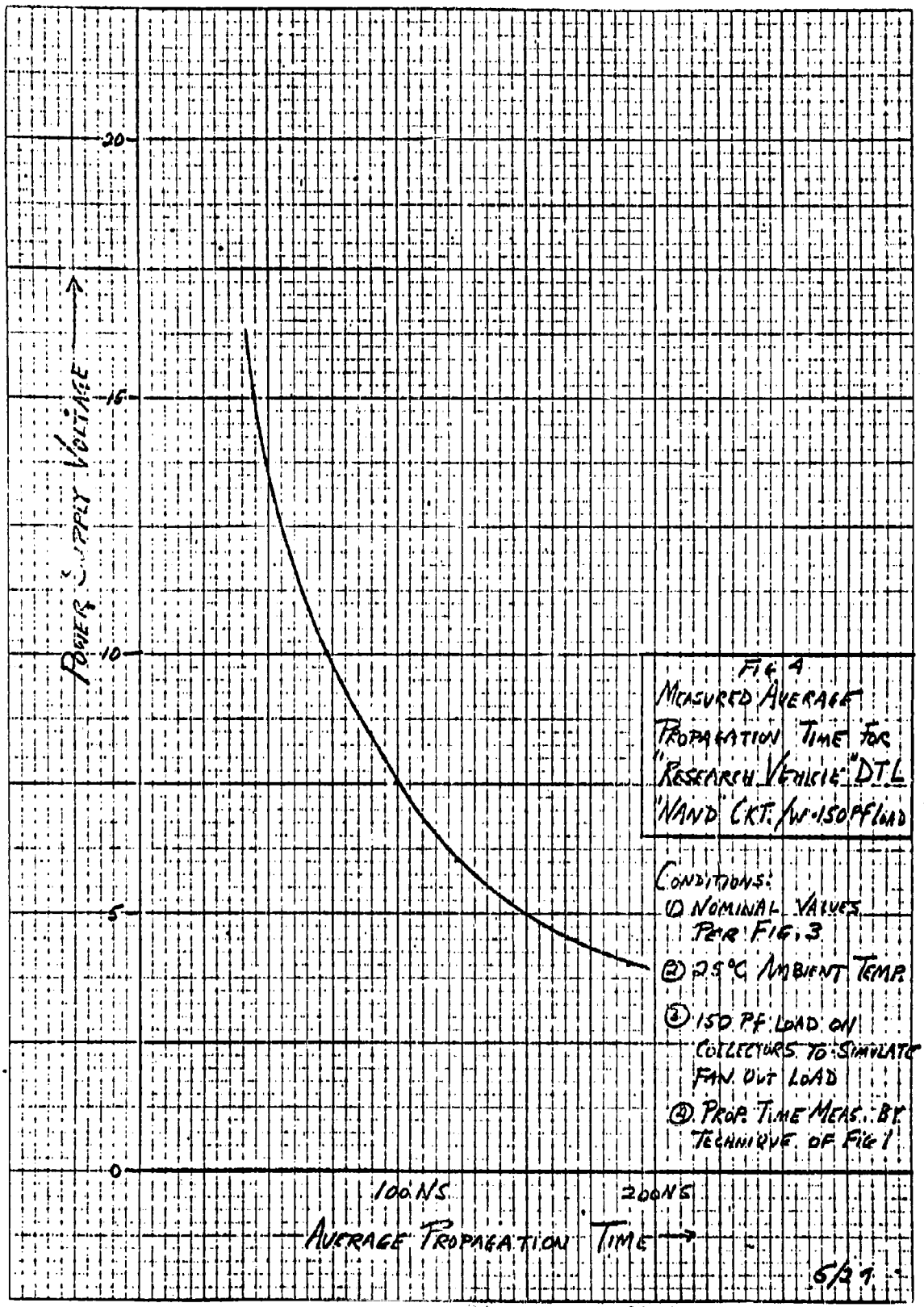


FIGURE 4

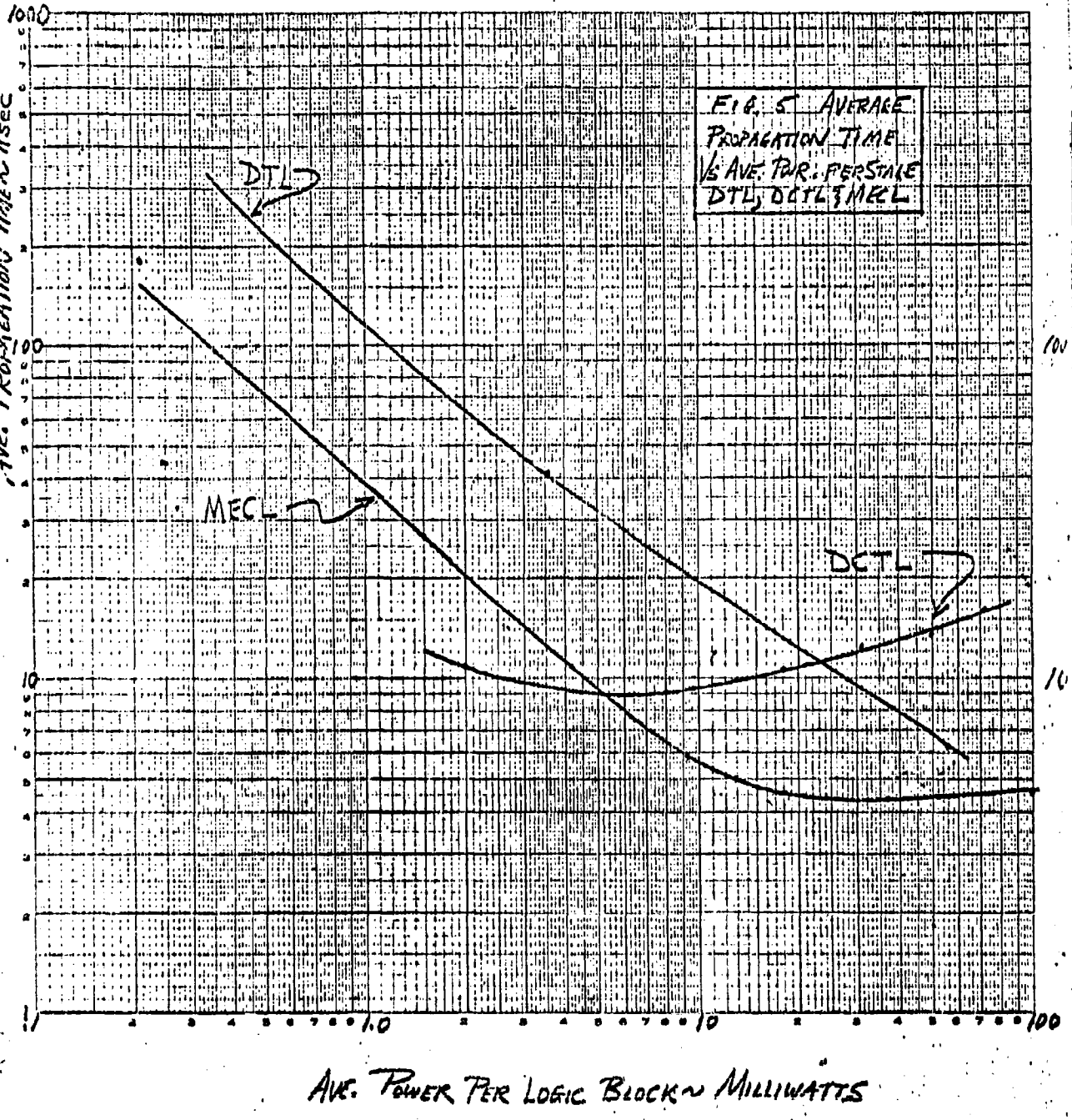


FIG. 5 AVERAGE PROPAGATION TIME VS AVE. POWER PER GATE DTL, DCTL & MECL
DTL
MECL
DCTL
AVE. PROPAGATION TIME n SEC
AVE. POWER PER LOGIC BLOCK ~ MILLIWATTS
1000
100
10
1.0
1.0
10
100

FIGURE 5

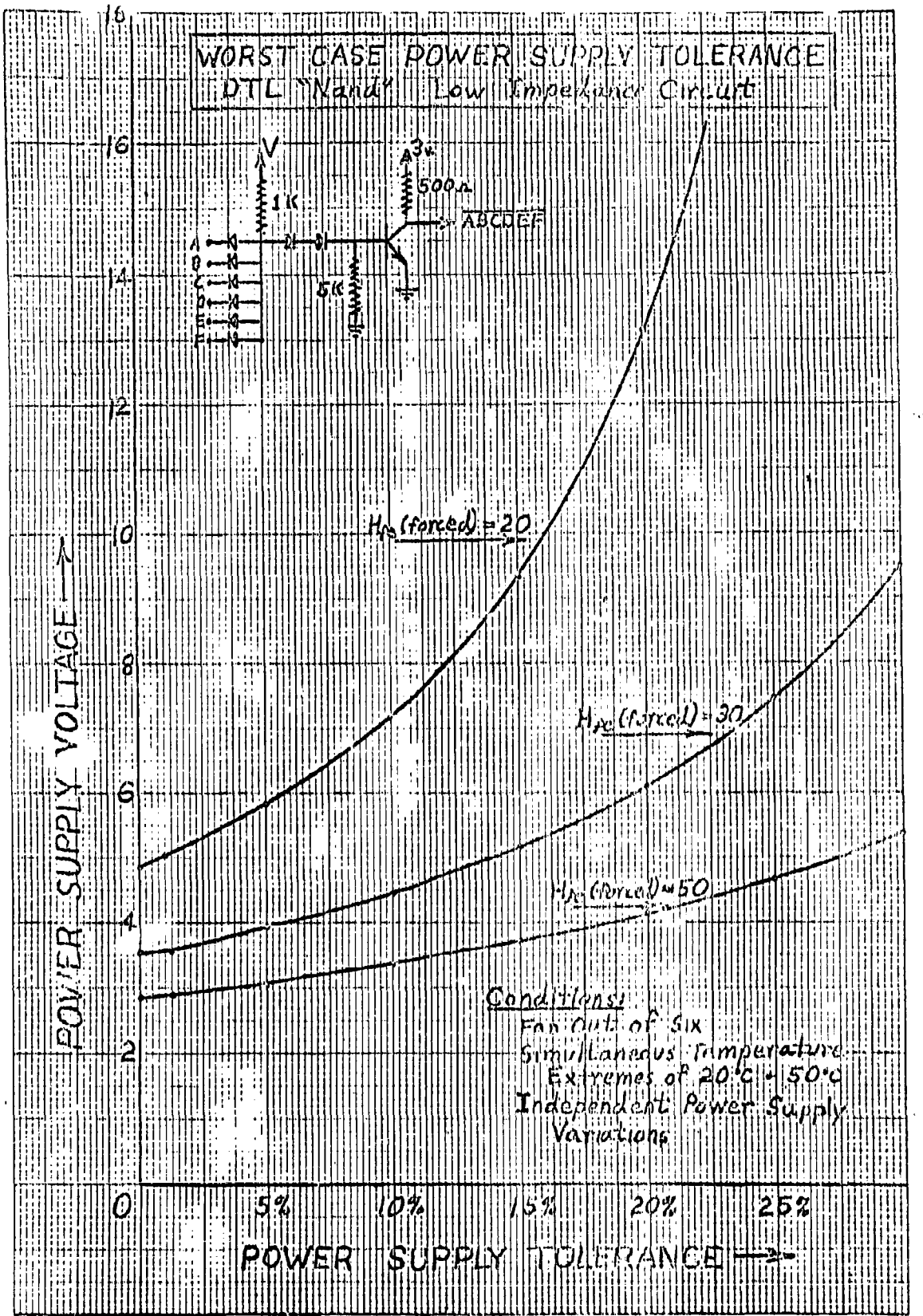

WORST CASE POWER SUPPLY TOLERANCE
DTL "Nand" Low Impedance Circuit
V
1K
3K
500Ω
ABCDEF
5K
POWER SUPPLY VOLTAGE
16
14
12
10
8
6
4
2
0
H_{FE} (forced) = 20
H_{FE} (forced) = 30
H_{FE} (forced) = 50
Conditions:
Fan out of six
Simultaneous Temperature Extremes of 20°C + 50°C
Independent Power Supply Variations
5%
10%
15%
20%
25%
POWER SUPPLY TOLERANCE

FIGURE 6

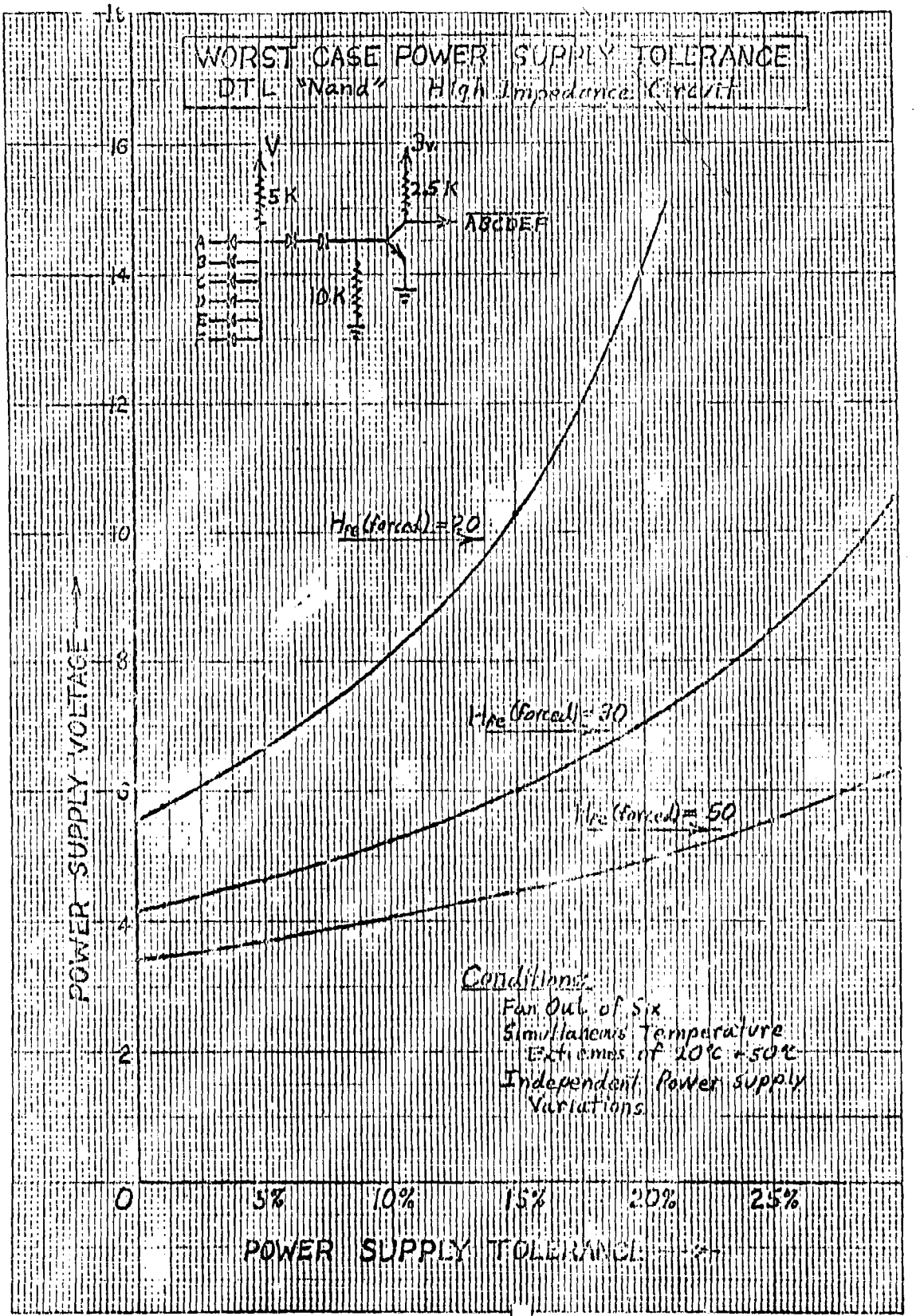

WORST CASE POWER SUPPLY TOLERANCE
DTL "Nand" High Impedance Circuit
V
5K
3v.
2.5K
ABCDEF
10K
POWER SUPPLY VOLTAGE
16
14
12
10
8
6
4
2
0
H_{FC} (forced) = 20
H_{FC} (forced) = 30
H_{FC} (forced) = 50
Conditions
Fan Out of Six
Simultaneous Temperature
Extremes of 20°C - 50°C
Independent Power Supply
Variations
5%
10%
15%
20%
25%
POWER SUPPLY TOLERANCE

FIGURE 7

ASSUMPTIONS IN WORST CASE ANALYSIS:

Use of 2N834 Type Transistor:

Average Base Resistance = 57Ω (allowing 10% spread) ∴ $R_{b_{max}} = 63\Omega$

$V_{BT}(sat) \simeq .73$ v. (allowing 10% spread; −.00235 volts/°C Temp Coeff.)

$V_{BT}(sat)$:	Max	Min
Warm (50°C)	.737v	.603v
Cool (20°C)	.814v	.666v

$V_{CE}(sat) \simeq .15$ v. (allowing 10% spread; +.00036 volt/°C Temp. Coeff.)

$V_{CE}(sat)$:	Max	Min
Warm (50°C)	.175v	.143v
Cool (20°C)	.163v	.133v

Input Diode:

Average Conducting Drop = .45volts (allowing 10% spread; −.002 volt/°C Temp. Coeff.)

V_{d_1}:	Max	Min
Warm (50°C)	.484v	.396v
Cool (20°C)	.55v	.45v

Base Drive Diodes:

Average Conducting Drop = .6 volts (allowing 10% spread; −.002 volt/°C Temp. Coeff.)

V_{d_2}:	Max	Min
Warm (50°C)	.649v	.531v
Cool (20°C)	.715v	.585v

Resistors:

- .1%/°C Temp Coefficient; Variation from Std Temp (25°C) to 20°C + 50°C
- ± 20% Resistivity error per wafer
- ± 2% Random Error within wafer

Low Impedance Circuit:

	STD. VALUE	Warm (80°C) Up 20% Wafer Max	Warm (80°C) Up 20% Wafer Min	Warm (80°C) Down 20% Wafer Max	Warm (80°C) Down 20% Wafer Min	Cool (20°C) Up 20% Wafer Max	Cool (20°C) Up 20% Wafer Min	Cool (20°C) Down 20% Wafer Max	Cool (20°C) Down 20% Wafer Min
R_1	1K	1.245K	1.205K	.845K	.805K	1.215K	1.175K	.815K	.775K
R_2	5K	6.23K	6.02K	4.23K	4.02K	6.08K	5.87K	4.08K	3.87K
R_3	500Ω	623Ω	602Ω	423Ω	402Ω	608Ω	587Ω	408Ω	387Ω

High Impedance Circuit:

	STD. VALUE	Warm (50°C) Up 20% Wafer Max	Warm (50°C) Up 20% Wafer Min	Warm (50°C) Down 20% Wafer Max	Warm (50°C) Down 20% Wafer Min	Cool (20°C) Up 20% Wafer Max	Cool (20°C) Up 20% Wafer Min	Cool (20°C) Down 20% Wafer Max	Cool (20°C) Down 20% Wafer Min
R_1	5K	6.225K	6.025K	4.225K	4.025K	6.075K	5.875K	4.075K	3.775K
R_2	10K	12.45K	12.05K	8.45K	8.05K	12.15K	11.75K	8.15K	7.75K
R_3	2.5K	3.113K	3.013K	2.113K	2.012K	3.038K	2.937K	2.04K	1.927K

FIGURE 8

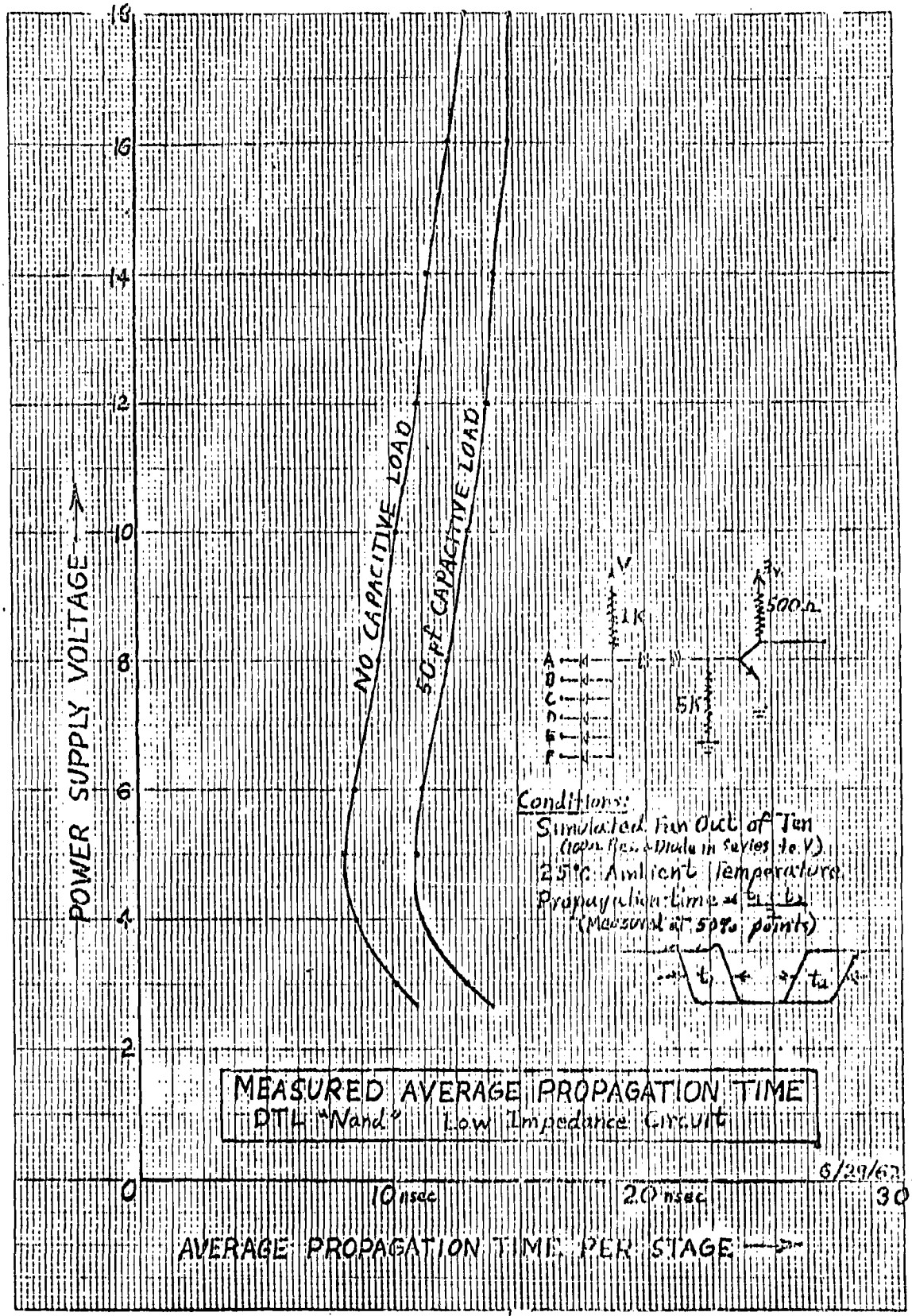

POWER SUPPLY VOLTAGE
16
14
12
10
8
6
4
2
0
NO CAPACITIVE LOAD
50 pf CAPACITIVE LOAD
1K
500Ω
5K
A
B
C
D
E
F
Conditions:
Simulated Fan Out of Ten
(Capacitive Diode in series to V)
25°C Ambient Temperature
Propagation time at t_a - t_b
(Measured at 50% points)
t_b
t_a
MEASURED AVERAGE PROPAGATION TIME
DTL "Nand" Low Impedance Circuit
6/29/62
10 nsec
20 nsec
30 nsec
AVERAGE PROPAGATION TIME PER STAGE

FIGURE 9

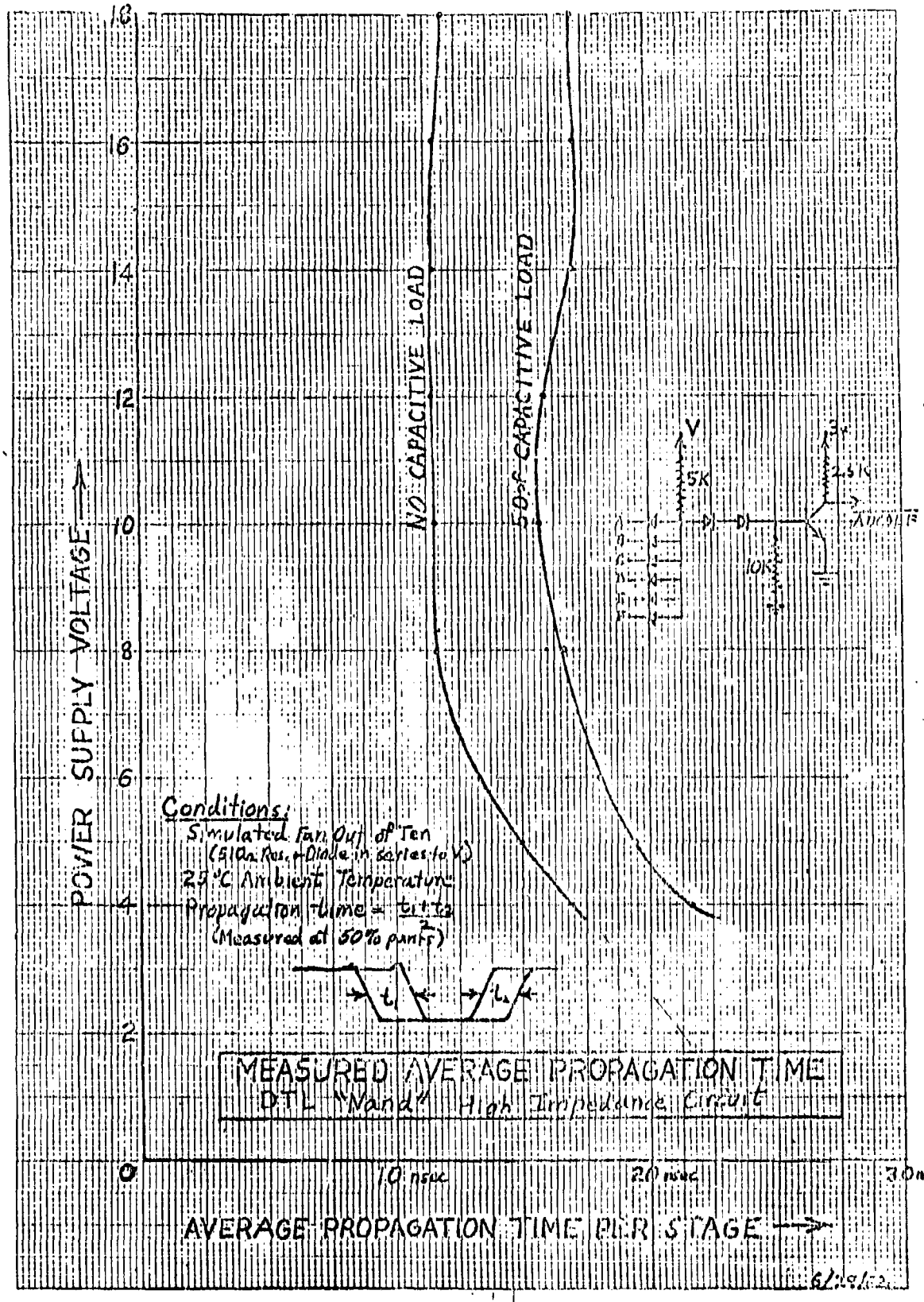

POWER SUPPLY VOLTAGE
NO CAPACITIVE LOAD
50 pF CAPACITIVE LOAD
Conditions:
Simulated Fan Out of Ten
(510Ω Res. + Diode in series to V)
25°C Ambient Temperature
Propagation Time = t1 + t2
(Measured at 50% points)
MEASURED AVERAGE PROPAGATION TIME
DTL "Nand" High Impedance Circuit
10 nsec
20 nsec
30 nsec
AVERAGE PROPAGATION TIME PER STAGE

FIGURE 10

CIRCUIT CONFIGURATIONS
For Proposed "Universal DTL Logic Package"

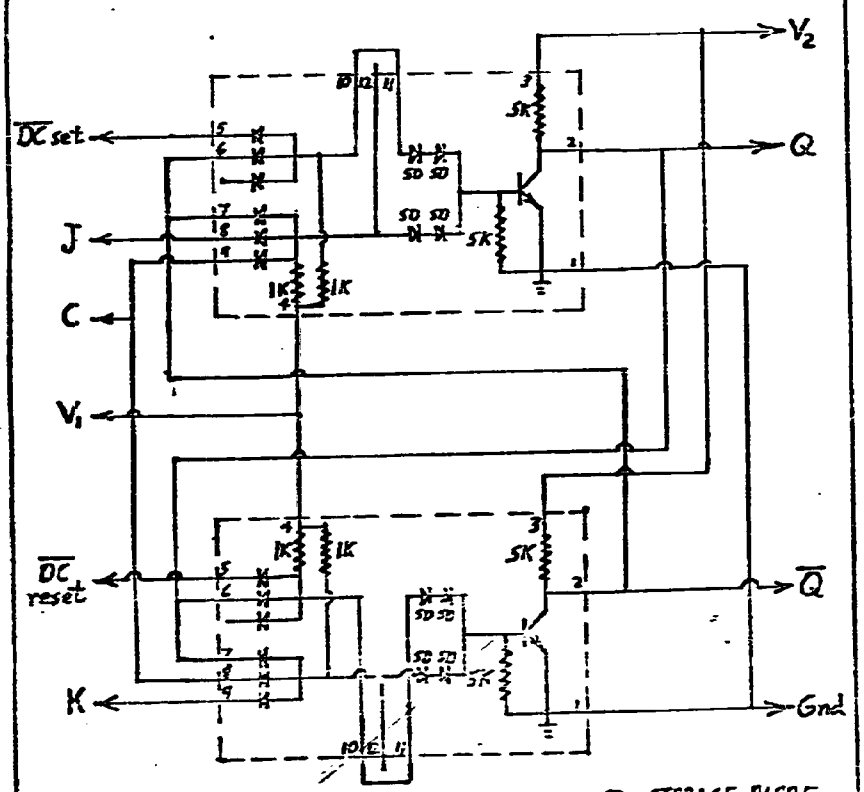


FIGURE 11

DTL TRAILING EDGE J-K-T FLIP-FLOP WITH D.C. RESET

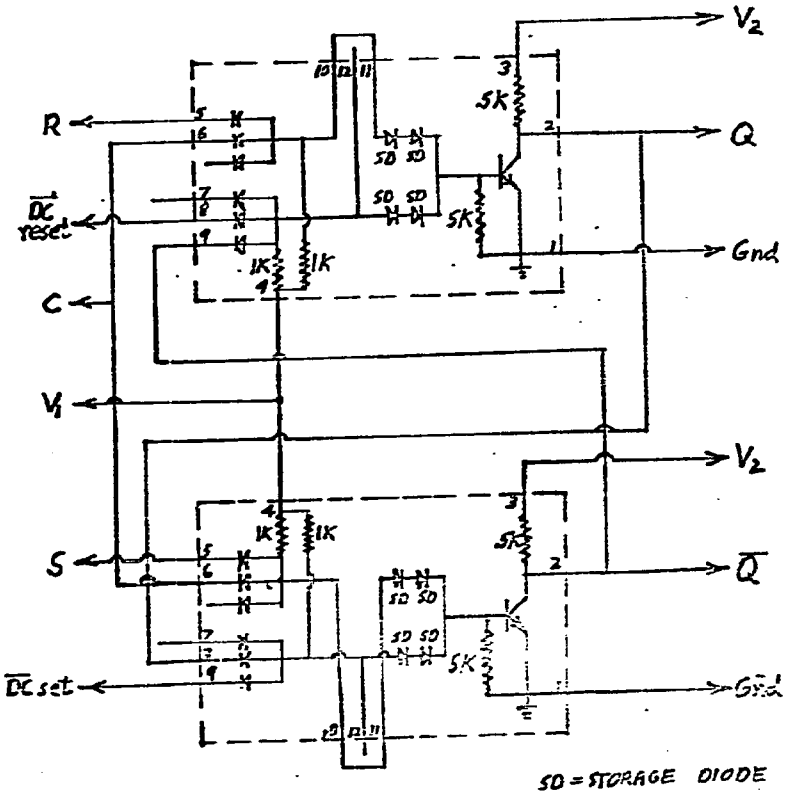


FIGURE 12

DTL LEADING EDGE R-S CLOCKED FLIP-FLOP WITH D.C. RESET

CIRCUIT CONFIGURATIONS CONT'D
For Proposed "Universal DTL Logic Package"

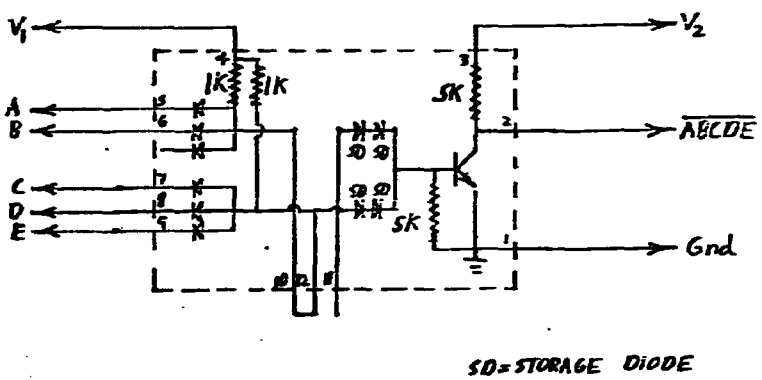


FIGURE 13
FIVE INPUT "NAND" CIRCUIT

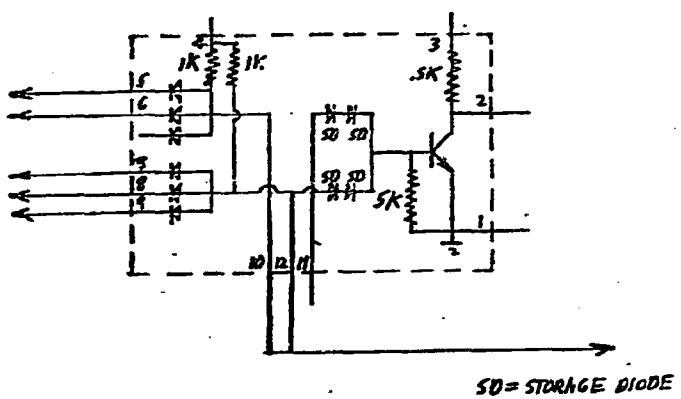


FIGURE 14
MULTIPLE DIODE ASSEMBLY

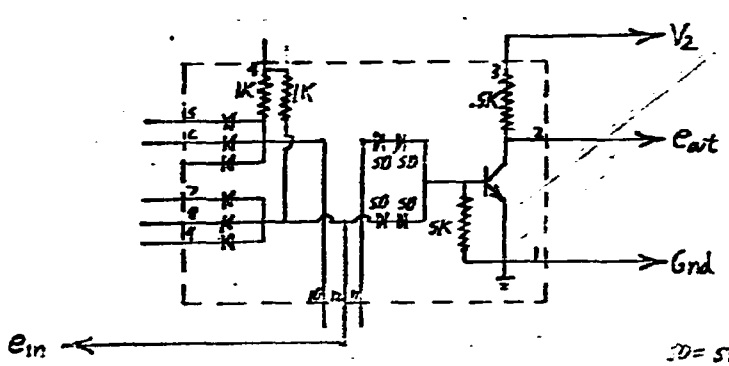


FIGURE 15
"NOISE PROTECTED"
INVERTER CIRCUIT

ALL DIODES OF FAST FD-100 TYPE UNLESS OTHERWISE STATED

6.0 UHF TRANSCEIVER DESIGN AND FABRICATION

6.1 Fabrication of Hybrid Integrated Circuits

The various hybrid integrated circuits for the transceiver have all been completely designed and most have been fabricated in sufficient numbers for several models. These include redesigns of several stages for various reasons. For example, the detector and AGC stages have been completely redesigned to eliminate some leakage currents which developed in the filter capacitor zener diodes, making the stages operate poorly in the receiver model.

Apparently, this increased leakage is due to partial degradation of the diode junction, due to partial alloying of gold with the silicon, during the strap-bonding process. A slight increase in leakage current is not especially intolerable in the case of the grounded bypass capacitors in the regular linear amplifier stages. In this particular case, the combination of the high value resistors in the AGC filter with the leakage current causes an objectionable load on the AGC signal.

The high frequency stages (120 Mc RF and 108 Mc Oscillator) have been redesigned around the new ultra high frequency transistor recently made available. This provides 10 db more RF gain and higher oscillator stability than in the original stages.

The new RF stages, including those in the transmitter section are being fabricated with the RF capacitors within the TO-5 can.

Some spiral inductors recently received from the Motorola Solid-State Division now appear to be able to withstand the required bonding temperatures, and some 108 Mc oscillator units are, at present, being built with integrated inductors in which the only outboard component will be the frequency controlling crystal.

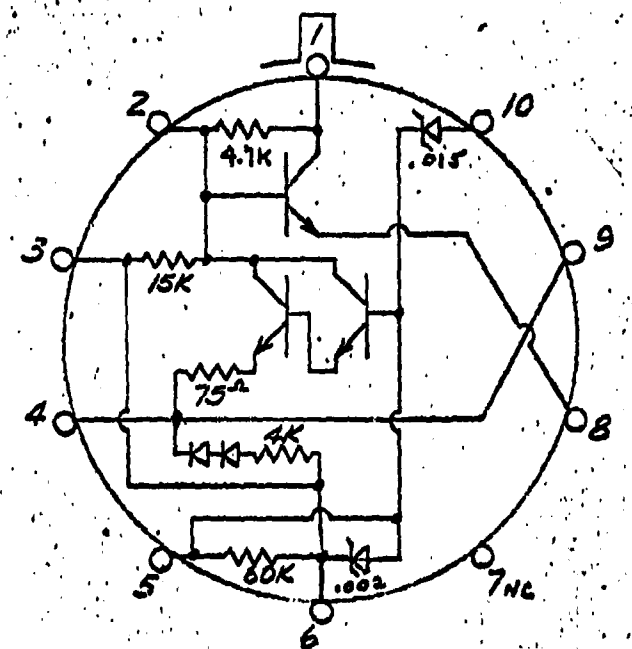
Some experiments are also underway in mounting some very small toroid inductors within the TO-5 can in association with a circuit.

The audio amplifier stage, which was described in a previous report, has proven to be unreliable from a fabrication standpoint. The problem appears to be that the Darlington voltage amplifier requires careful balance of the input base bias. Since our best resistor tolerance at this time is $\pm 10\%$, with some local variations outside of this limit, this delicate bias adjustment is not always obtained, resulting in a large percentage of stages with poor operational characteristics.

It has appeared worthwhile to redesign this stage also. A similar less critical circuit has been developed which will be more reproducible, and provide better gain with less distortion. This stage will include a direct output into the new offset receiver transducers recently received. This approach eliminates the necessity for a large coupling capacitor from the audio output into the speaker.

A schematic diagram of the improved audio amplifier is shown in Figure 1.

627 AUDIO AMP. REDESIGN



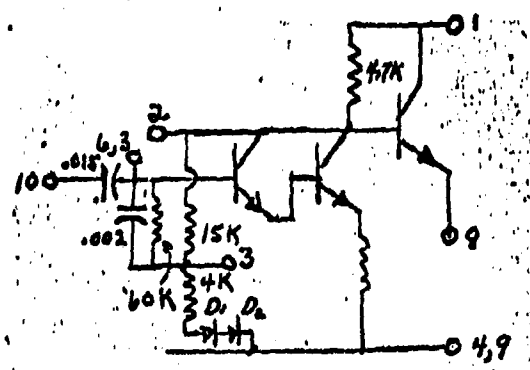


FIGURE 1

Redesigned AF Amplifier for Direct Coupled Offset Speakers.

6.2 Crystal Filters

One of each of the 120 Mc and 12 Mc crystal filters have been received from the Chicago Motorola Communications Division. These units have the four-crystal filter network mounted in TO-5 cans, but other components, such as resistors, capacitors and toroid inductors are mounted outboard. We are conferring with the supplier on the possibilities of either further concentration of elements, a slightly larger container, or a two-can all-internal mounting.

In all respects, these filters operate very well, and have been added to the interim circuit board model.

6.3 Inductor Development and Other New Hybrid Circuit Elements

Inductors for the hybrid integrated circuits so far developed all take the form of a spiral deposition of metal on a ceramic substrate. This substrate occupies one layer on the TO-5 ten pin header.

These are made by the Motorola Solid-State Systems Division by thin film, masking and gold deposition techniques. In the first samples received, the metallization lifted off the highly polished ceramic substrate in the wire bonding procedure at the temperature of 350°C. Later samples made on unpolished ceramics have proved more temperature stable, and these will probably be suitable for integration into the cans.

Some experimental inductors were made in our own facility by a silk screening process. These have excellent adherence to

the ceramic, due to the sintered moly-manganese metallization. Evaluation has shown that these have only an average of .03 uh. This is due to the very wide spacing between turns, required by the tolerances presently available in the silk screening technique. These are not, at the present time, suitable for use in the transceiver.

Several relatively new elements for hybrid integrated circuit structures have been developed. These include the dielectric capacitors. These capacitors are formed on very low resistivity silicon substrate with oxide coating. The upper capacitor plates are deposited aluminum. In one form called the binary capacitor, areas are increasing by doubling, which can provide any capacitance between 2 and 254 pfd in increments of 2 pfd, by suitably connecting the top plates.

These capacitors are especially useful in high frequency circuits, where junction capacitors, such as the zener diodes or other p-n junction areas will not perform satisfactorily.

A photograph of the top layer of the redesigned 120 Mc Mixer stage (624) using the new UHF transistors and binary capacitors is given in Figure 2.

The UHF transistor is a new design which provides a f_T cutoff frequency of 1000 Mc or more. This provides much more gain and better performance in high frequency applications than the 2N834 UHF transistor used up to the present time.

Another new element is the planar passivated zener diode. This device will have several advantages over the standard zener

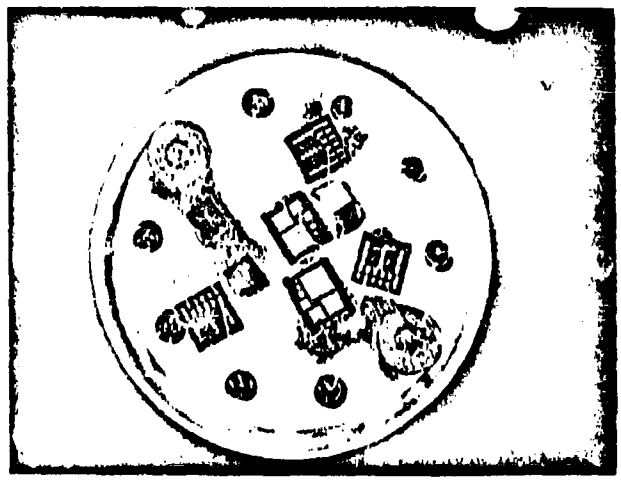


FIGURE 2

Redesigned 624; 120 Mc RF mixer stage including UHF transistors and binary RF capacitors.

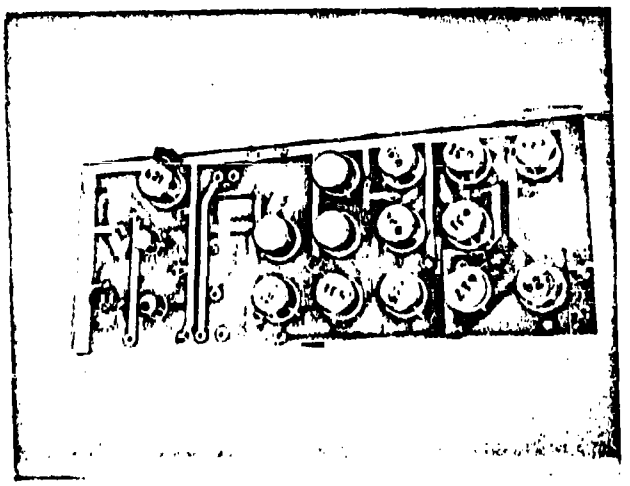


FIGURE 3

Partly assembled interim model Transceiver Circuit Board

diode dies presently used in hybrid integrated circuits. The oxide passivation will, of course, provide cleaner units in all cases, and the aluminum metallization will provide bonding without the risk of gold alloying. These will be provided for fabrication of hybrid integrated circuits in the near future.

An additional new electronic component is the offset high impedance miniature speaker. This has been designed by the vendor for coupling directly into the audio output circuit, thus, eliminating the 5 ufd coupling capacitor. The DC amplifier current pulls the diaphragm to the center and allows full diaphragm excursion without any limiting.

6.4 Interim Model Transceiver

Circuit boards and a containing package to house a complete transceiver model has been designed and the hardware fabricated. The package includes all peripheral equipment, batteries and collapsible dipole antenna.

One model has been assembled on this structure. At present, this model contains the complete receiver section and the transmitter section will be installed very shortly.

In the assembly on the circuit board, shown in Figure 3 hybrid integrated circuits are used throughout. Some of these stages, notably the RF and crystal filter stages require some outboard components. New designs of some of these units as

discussed elsewhere in this report, will greatly reduce this load of exterior components.

These new hybrid integrated stages will be designed onto a new circuit board with reduced dimensions. This latter design will be then approaching the final model.

Further reductions in size may be effected when single block integrated amplifiers and other circuits become available. The overall size factor may be substantially improved by the adoption of the new flat package which has been proposed.

6.5 Hybrid Integrated Linear Amplifier

The fabrication experience of the hybrid integrated circuit units for this transceiver development, has indicated that certain of these units can be produced with a relatively high degree of reproducibility. This is especially true of several of the units used as IF amplifiers in both the 12 Mc and 455 Kc sections.

These units may be cascaded together along with crystal or ceramic resonant filter elements to provide IF amplifier strips at several useful conventional frequencies.

Since such strips may be of quite wide interest in many areas, some preliminary evaluations have been made on these cascaded amplifier strips.

Two hybrid integrated linear amplifier circuits we have developed, appear to be useful on a general purpose IF application basis. These are:

(1) The H.I.C. 640 Fixed Bias Stage as shown schematically in Figure 4. This is a perfectly conventional voltage amplifier stage with built-in emitter bypass and both direct and capacative collector outputs available.

(2) The H.I.C. 631 stage, provides the same features, in addition to an isolated base input network for the injection of a D.C. bias voltage from an external source. This external source may be derived from a volume control, A.G.C., or other sources.

At maximum gain (about 1.5 volts positive on the injection network), this stage has essentially the same frequency and gain characteristics of the H.I.C. 640.

Some of the performance characteristics so far evaluated on cascaded strip amplifiers composed of these units are summarized in Figures 5 and 6.

Figure 5 shows the gain vs frequency for a single 640 stage when loaded with a following, cascaded 640 stage.

In this curve the low frequency fall off is due to the limiting aspects of the emitter bypass capacitor value. In the region of 455 Kc to 1 Mc the per-stage gain is better than 25 db, falling off to 11 db at 10 Mc. Anywhere in this region the gain is sufficient to be useful in practical IF amplifier strips.

Figure 6 shows the overall response of a two-stage IF amplifier with a series resonant ceramic 455 Kc filter. The H.I.C. schematic of this circuit is also shown. The 661 stage is a commercial ceramic resonant filter which has been mounted in a TO-5 can.

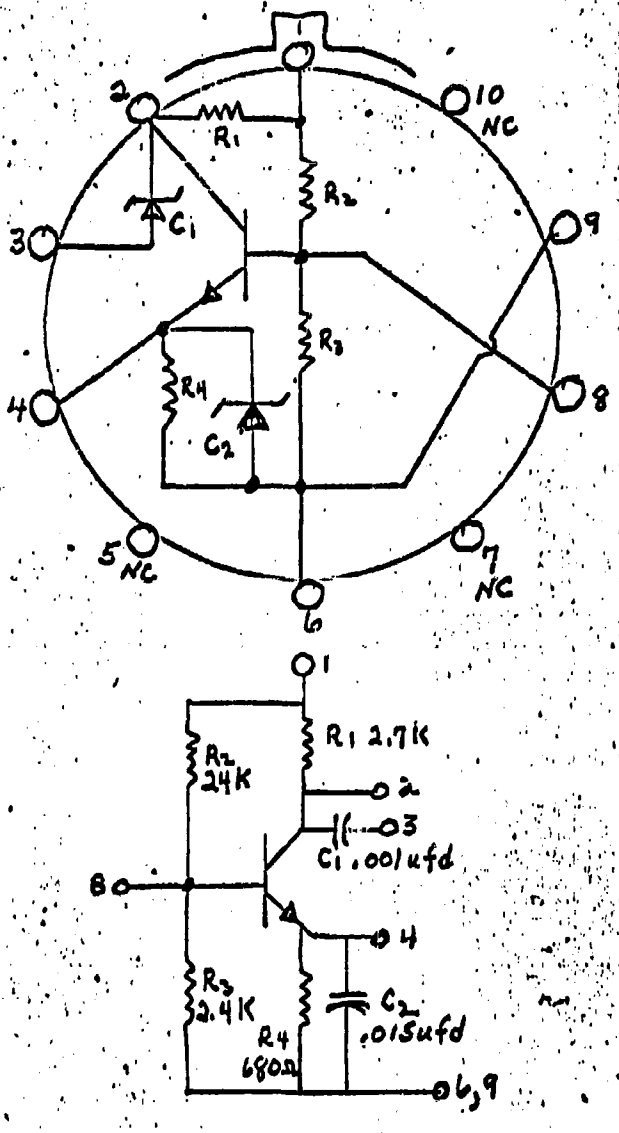


FIGURE 4

H.I.C. 640 Broad Band Linear RF Amplifier With Fixed Bias.

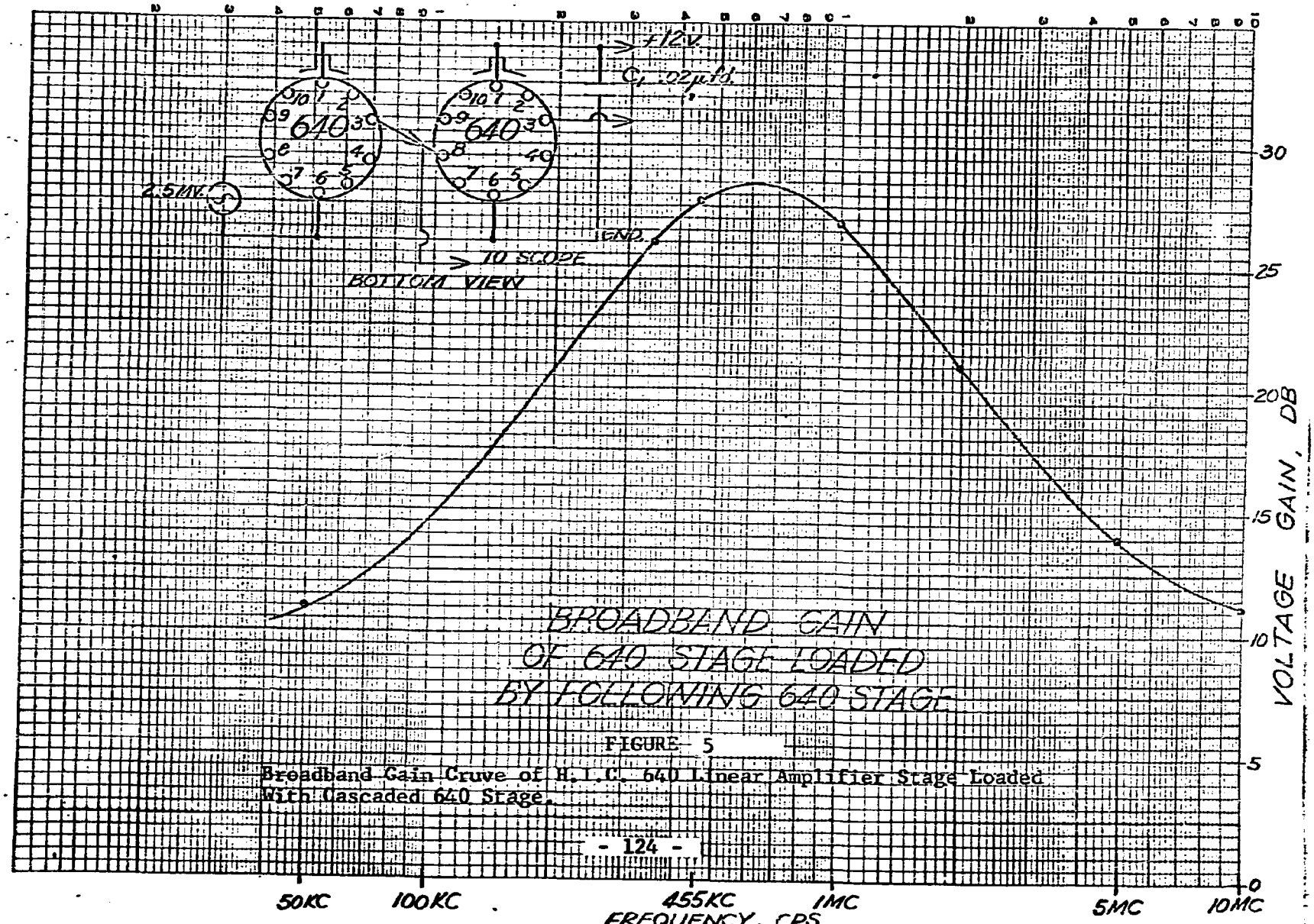


FIGURE 5

Broadband Gain Cruve of H. I. C. 640 Linear Amplifier Stage Loaded With Cascaded 640 Stage.

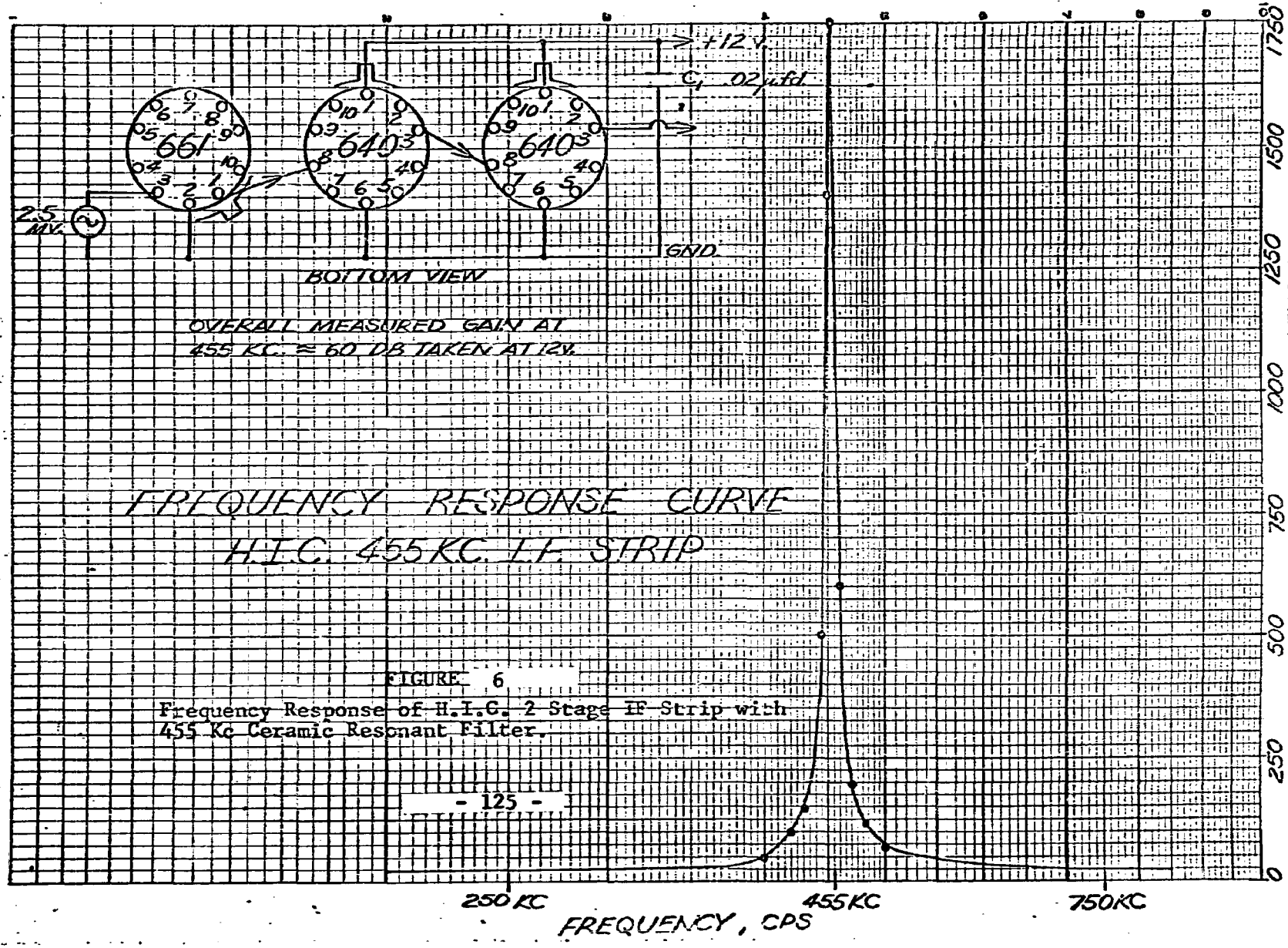


FIGURE 6

Frequency Response of H.I.C. 2 Stage IF Strip with 455 Kc Ceramic Resonant Filter.

A signal of 2.5 millivolts was used at the filter input. The maximum gain at 455 Kc was about 57 db. This closely agrees with the measured loaded gain of 28 db per stage, as indicated in the curve of Figure 5.

Some further evaluations of these amplifier strips at other IF frequencies will be completed in the near future.

6.6 Status of Hybrid Integrated Transreceiver Circuits

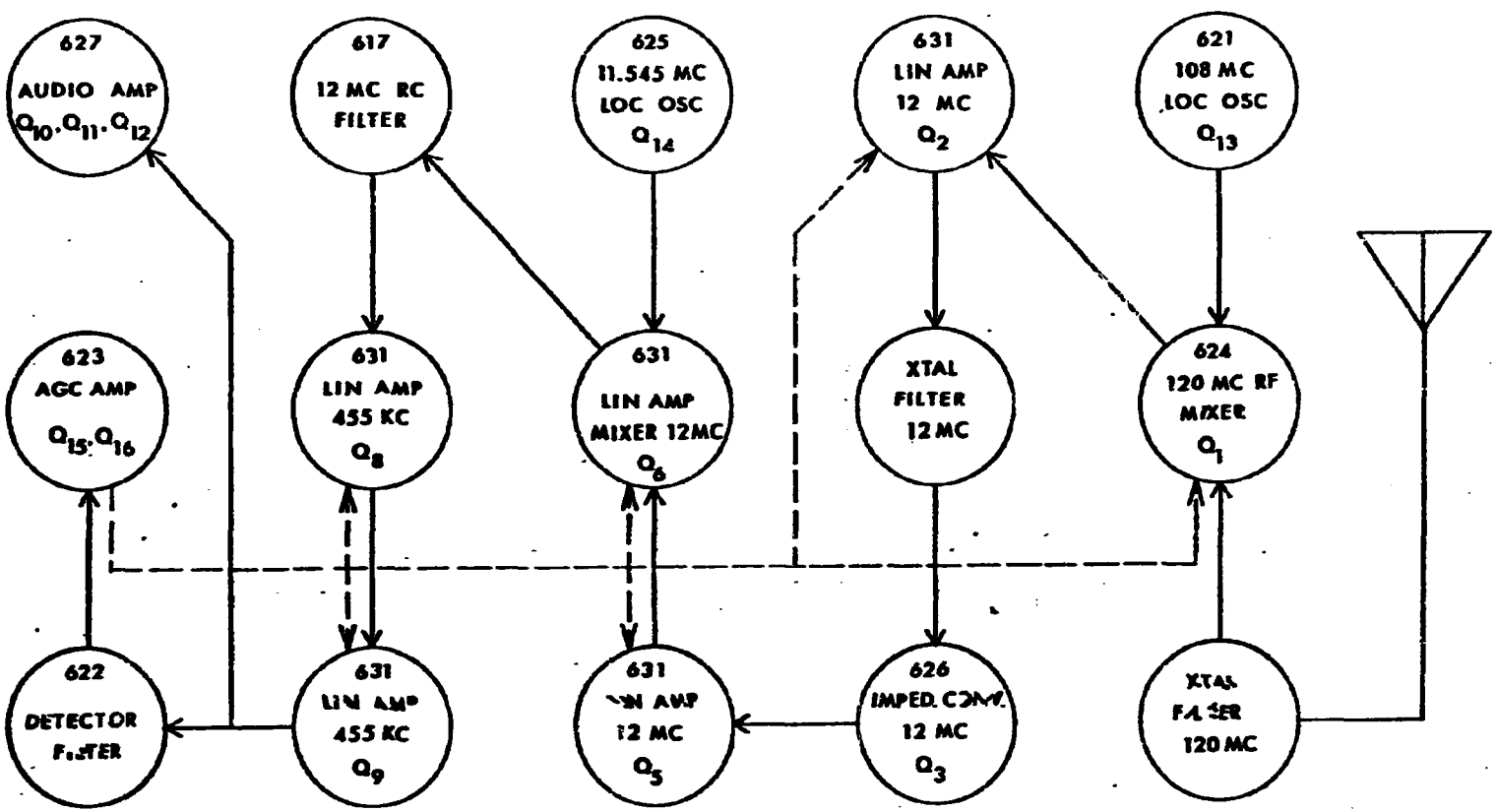
Sufficient quantities of all of the Hybrid Integrated Circuits to construct several UHF Transreceivers have been fabricated and tested. The designs are as near finalization as they can be made at this time pending the ultimate availability of certain other structural components and techniques. These include:

1. High Q high frequency capacitors
2. Passivated Zener diode capacitors in the large value ranges
3. Finalization of aluminum bonding process
4. Low value (50Ω/square) diffused resistors

The lack of these processes and elements has made it necessary to assemble the transreceiver models with several types of elements not mounted in the TO-5 can.

The present status of this assembly is summarized below.

The receiver section is shown in block diagram form in Figure 7. This 15 - TO-5 can circuit contains two crystal filter stages and 13 hybrid integrated circuits. These circuits have



BLOCK DIAGRAM

120 MC AM RECEIVER

Figure 7

code numbers which identify them for their function in the transreceiver.

The schematic diagrams of these H.I.C. units are shown with pin connections in Figures 8 and 9. Outboard elements in these schematics are shown connected with arrows. (⟷).

The following circuits are completely integrated in hybrid form:

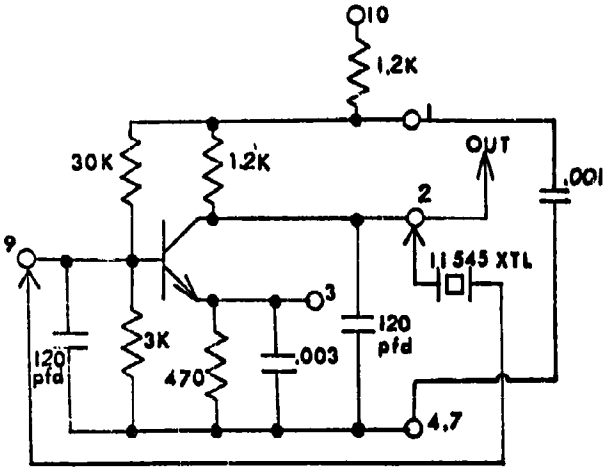
631 - 12 Mc and 455 Kc Linear Amplifier
622 - Detector Filter
623 - AGC Amplifier
627 - Audio Amplifier
617 - 12 Mc RC Filter
626 - 12 Mc Impedance Converter

In the other stages:

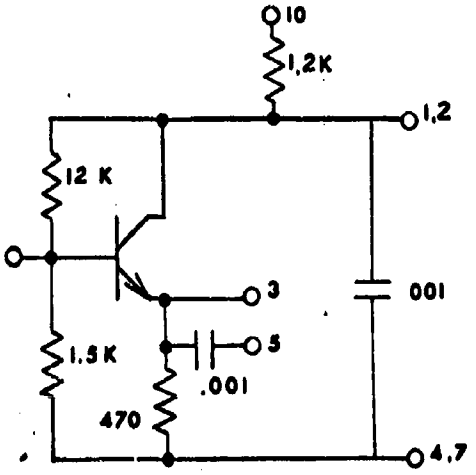
625 - The 11.545 Mc local oscillator is complete except for outboard crystal
621 - 108 Mc local oscillator requires two toroid inductors, one crystal, one trimmer capacitor and two high Q glass capacitors mounted outboard

Similarly, the 624 requires two toroids, and four high Q capacitors mounted outboard.

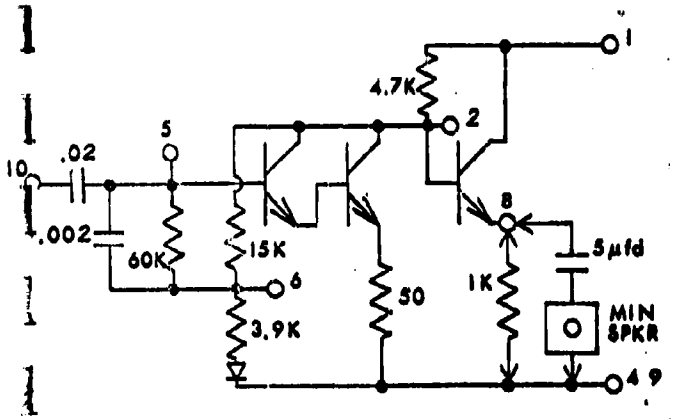
In all of these hybrid mounts, standard production zener diode dies are being used as filter, bypass, and coupling



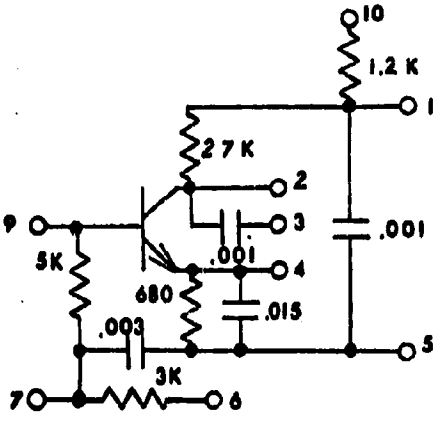
625 11.545 LOCAL OSCILLATOR



626 IMPED. CONV., 12 MC

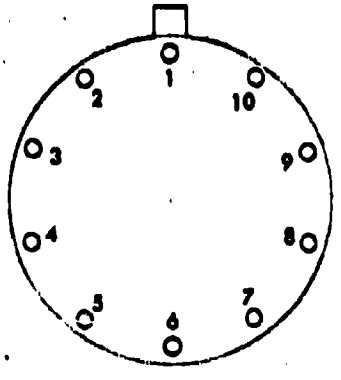


627 AUDIO AMP



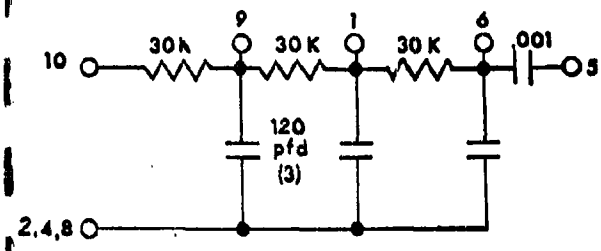
631 LINEAR AMP WITH AGC INPUT 12 MC AND 455 KC

NOTE: NUMBERED TERMINALS ARE PIN NO'S ON TO-5 10 PIN HEADER.
UNLESS OTHERWISE NOTED:
RESISTANCE GIVEN IN Ω
CAPACITANCE GIVEN IN µfd

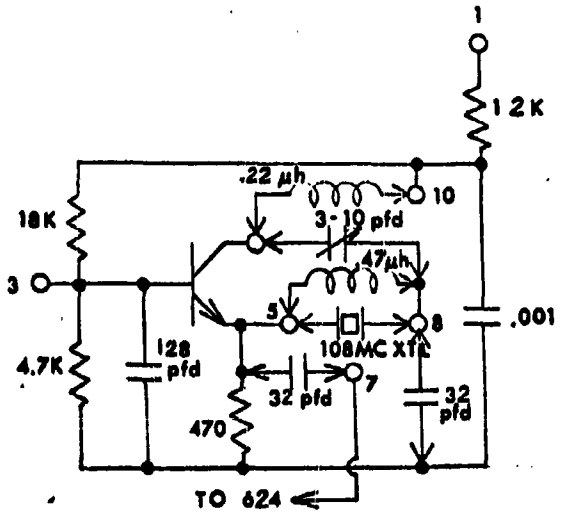


TO-5 10 PIN H.I.C. MODULE TOP VIEW

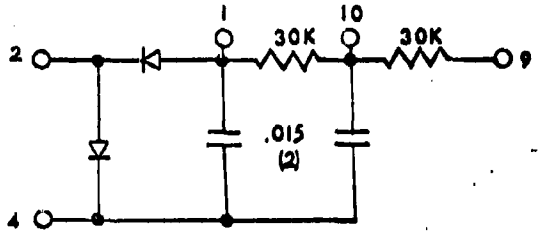
Figure 8



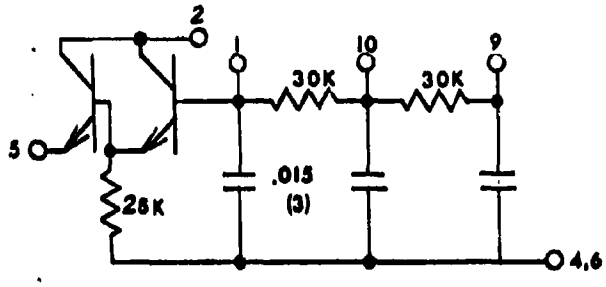
617 12 MC RC FILTER



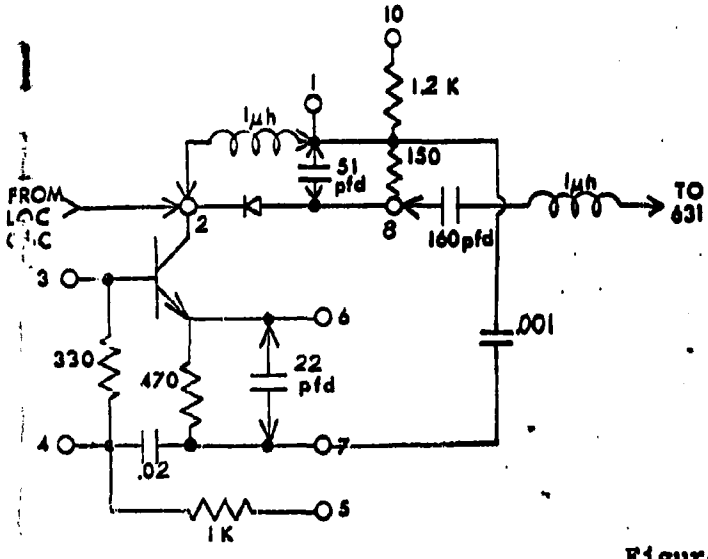
621 108 MC LOCAL OSC



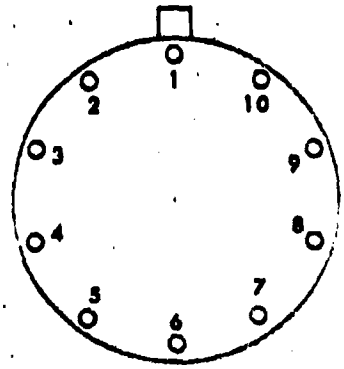
622 DETECTOR & FILTER



623 AGC AMP



624 120 MC RF MIXER



TO-5 10 PIN H.I.C. MODULE
TOP VIEW

Figure 9

capacitors. In most cases, these are satisfactory, but the over-all efficiency will be improved when the total range of passivated zener dies in the 623 A.G.C., the filter Amplifier, is troublesome. This will be greatly improved with the new components.

6.7 H.I.C. Fabrication Techniques

The reliable fabrication of the submount structures, i.e. the filter, bypass and coupling zener diode capacitors has been a problem. Bonding straps used in the earlier mounts failed in many cases, basically due to thermal stresses.

The ceramic sandwich mounting, briefly described in the last report, has proven a reliable and easily fabricated structure. A system of top and bottom ceramic metallization patterns has been developed, such that the large .090 and .135 inch zener dies can be mounted on any pin combination.

A 631 linear amplifier mount with three sandwiched diodes in the sublevels is shown in Figure 10.

Some of these mounts have been subjected to preliminary environmental tests including shock and centrifuge with excellent results. Additional data will be published when the tests are completed.

A further over-all improvement in the H.I.C. fabrication will result when the aluminum wire bonding becomes available. This will improve the bond reliability, as well as the thermal properties. This will also allow sublevel assembly of wire bonded circuits, not feasible now with gold wire bonding.

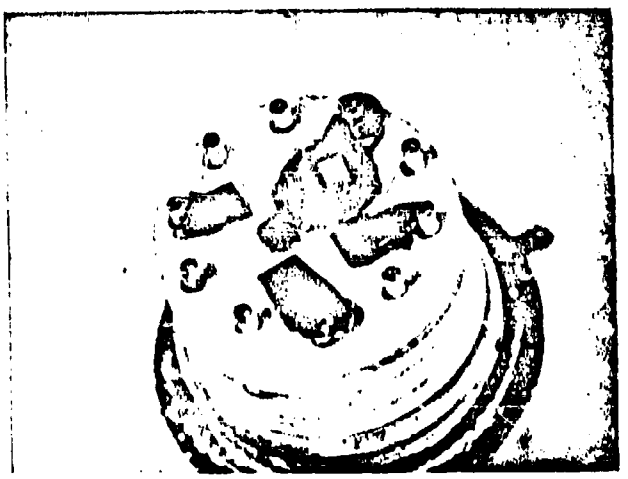


Figure 10

H.I.C. 631 Linear Amplifier with Ceramic Sandwich Construction

6.8 Transreceiver Model Construction

Two working models of the receiver part of the transreceiver and one working transmitter section have been assembled. These were made on the older circuit boards. There have been some biasing changes in the newer improved H.I.C. units and a new circuit board layout accommodating these changes has been designed. With these new boards, which will be available in a few days, the straightforward and clean construction of the H.I.C. parts of several models can be undertaken.

A temporary bottleneck appears to have developed in the crystal filter area. The structure, which includes four crystals in one TO-5 can, is apparently very difficult to fabricate and one extra can will be required for the peripheral input and output matching networks. This situation is now being resolved with our Chicago Motorola Applied Research Division.

In the newer models of the transreceiver, the new FEB amplifier circuits will be used in a minimum of two places for the 11.545 Mc local oscillator and the 12 Mc crystal filter driver buffer amplifier. A schematic diagram of the constitution of this oscillator with an outboard crystal and capacitor is given in Figure 11. This capacitor will be hybrid integrated in other models. These could be used in all of the IF stages also, except that the AGC system would have to be radically modified. It is anticipated that in the very near future, a transreceiver model using the FEB circuits in eight or nine stages can be designed. Ultimately, of course, all stages will be made in this way. This will include the adaption to a flat package with consequent radical reduction in circuit volume.

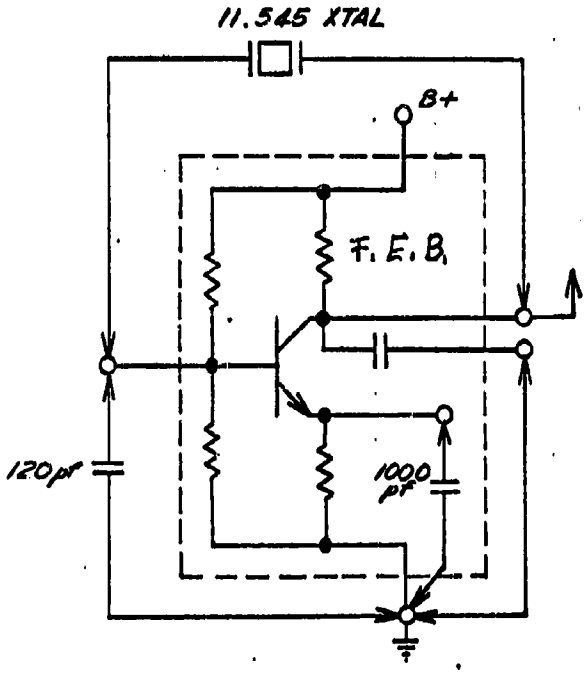


Figure 11

11.545 Mc Local Osc. as USED IN TRANSCRECEIVER
Model with F.E.B. AMPLIFIER

6.9 FEB Linear Amplifiers

The new FEB double linear amplifier was described briefly in the last report. Since then, further evaluations have been made and some practical mounts in TO-5 cans have been fabricated. Some of these have been incorporated in the transreceiver models.

The FEB amplifier, shown both in layout and in the equivalent schematic circuit, has been reproduced here for convenience in Figure 12. These have been mounted into TO-5 cans in three ways for evaluation and use in transreceiver circuits.

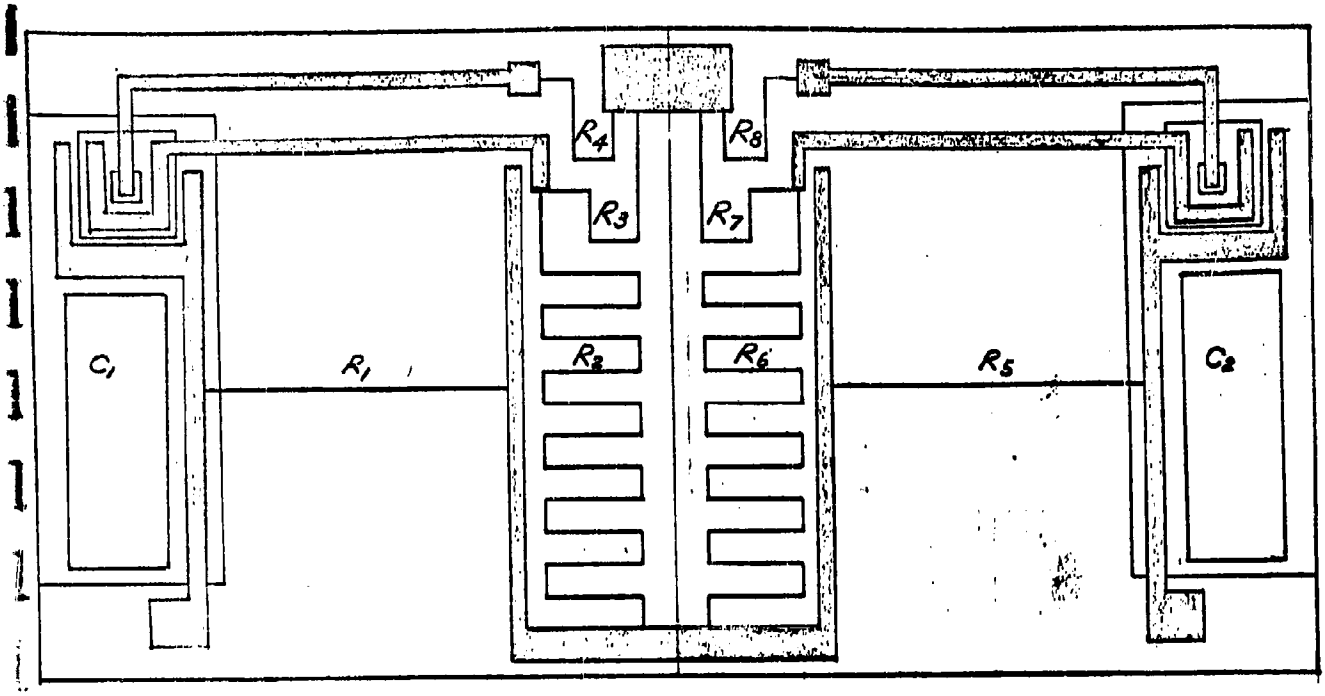
In 761 (Figure 13) the FEB has been mounted with all terminals brought out. This is used with external bypass capacitors, etc,, mostly in evaluation studies.

In 763 (Figure 14) consists of the same FEB and two 10,000 pf zener capacitors hybrid mounted in the same TO-5 can. This stage can be used cascaded for a high gain broadband amplifier.

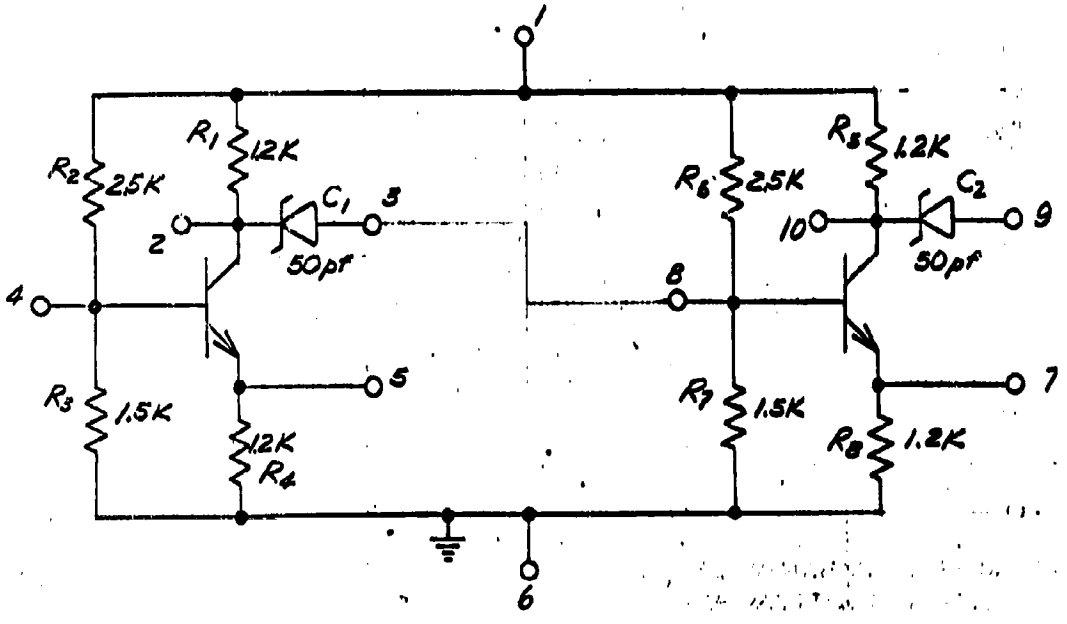
In 764 some of the FEB circuits either through breakage, metallization failure, etc., had only one good operating side. These have been mounted in TO-5 cans with 1000 pf zener emitter bypass, as shown in Figure 15.

The basing adapted in this model conforms to that of the 631 HIC linear amplifier stage and can be used on the same circuit board.

Some further characterizations of this amplifier have been made and these are summarized in the referred curves.



A. INTEGRATED LINEAR AMPLIFIER



B. CONVENTIONAL SCHEMATIC

FIGURE 12

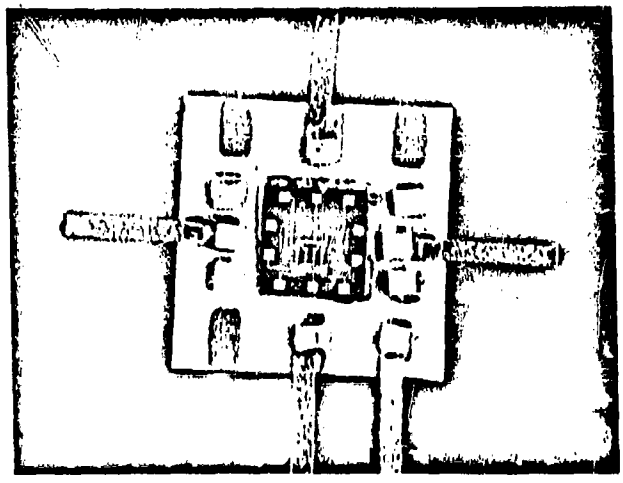


Figure 13

761 REB DUAL
(2-STAGE) LINEAR AMPLIFIER

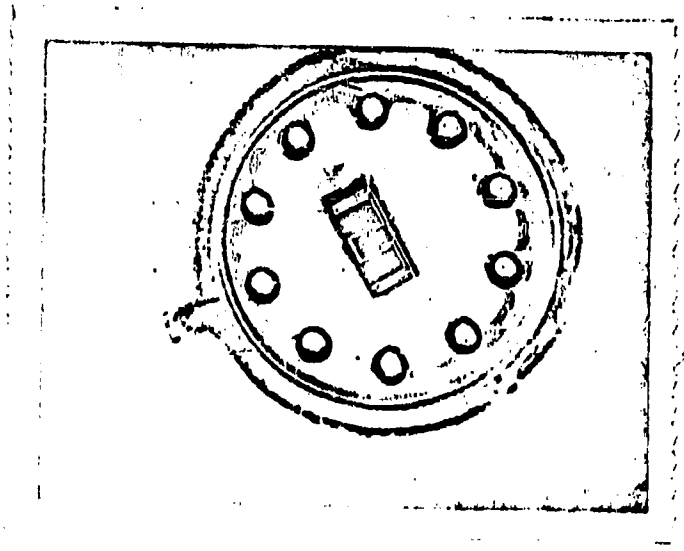


Figure 14

761 F.E.B. DUAL
(2-STAGE) LINEAR AMPLIFIER IN
TO-5 CAN

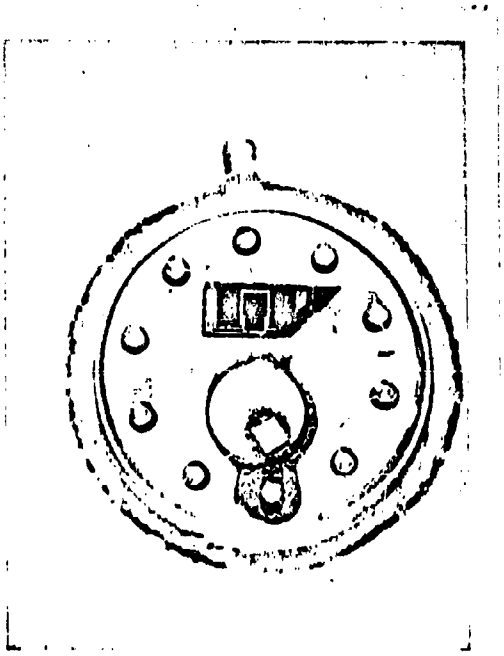


Figure 15
764 F.E.B. AMPLIFIER,
ONE SIDE ONLY, WITH 1000 pfd EMITTER
BYPASS CAPACITOR

The broadband voltage gain of a single FEB stage (one side only) from several different units is given in Figure 16. These curves show the voltage gain in db as measured from 455 Kc to 50 Mc. External emitter bypass of 10,000 pfd was used.

Figure 17 is the measured voltage gain for a complete FEB amplifier with coupling from the collector capacitor of the left stage to the base input of the right stage. This gain can be made about 6 db more, especially at the lower frequencies by using a 50 pfd external coupling capacitor. The reasons why the internal capacitors do not perform better are being investigated. The loaded matched power gain for two single side units with 10,000 pf emitter bypass is plotted in Figure 18.

The reverse gain for four units has been plotted in Figure 19. This indicates the amount of circuit feedback which may be troublesome in cascaded amplifiers.

The Y_{11} parametric measurements over a range of frequencies are shown in Figure 20 for two single amplifier units, and finally the Y_{22} parameters for the same two units are plotted in Figure 21.

Further evaluations are being made on available units.

These evaluations have pointed up a rather good reproducibility within the fabrication process. Also, evident are the very good frequency response and indicated absence of parasitics. With this and other information to be gathered later, it is believed a very useful FEB broadband linear amplifier, including emitter bypass and collector isolation filter circuits, can be designed. A consideration is being given to provide means for a variable base bias for AGC applications.

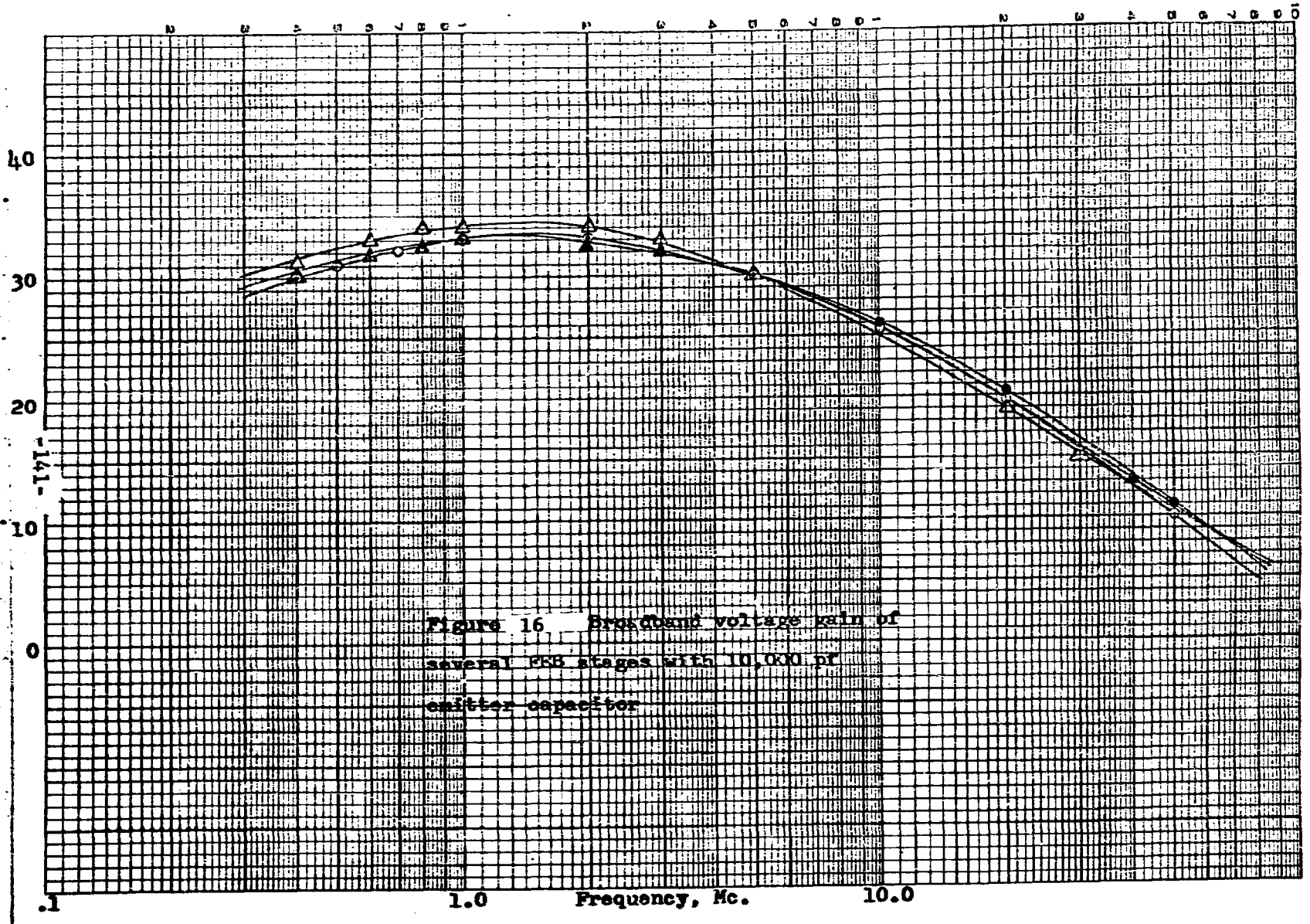


Figure 16. Broadband voltage gain of several FEB stages with 10,000 pf emitter capacitor

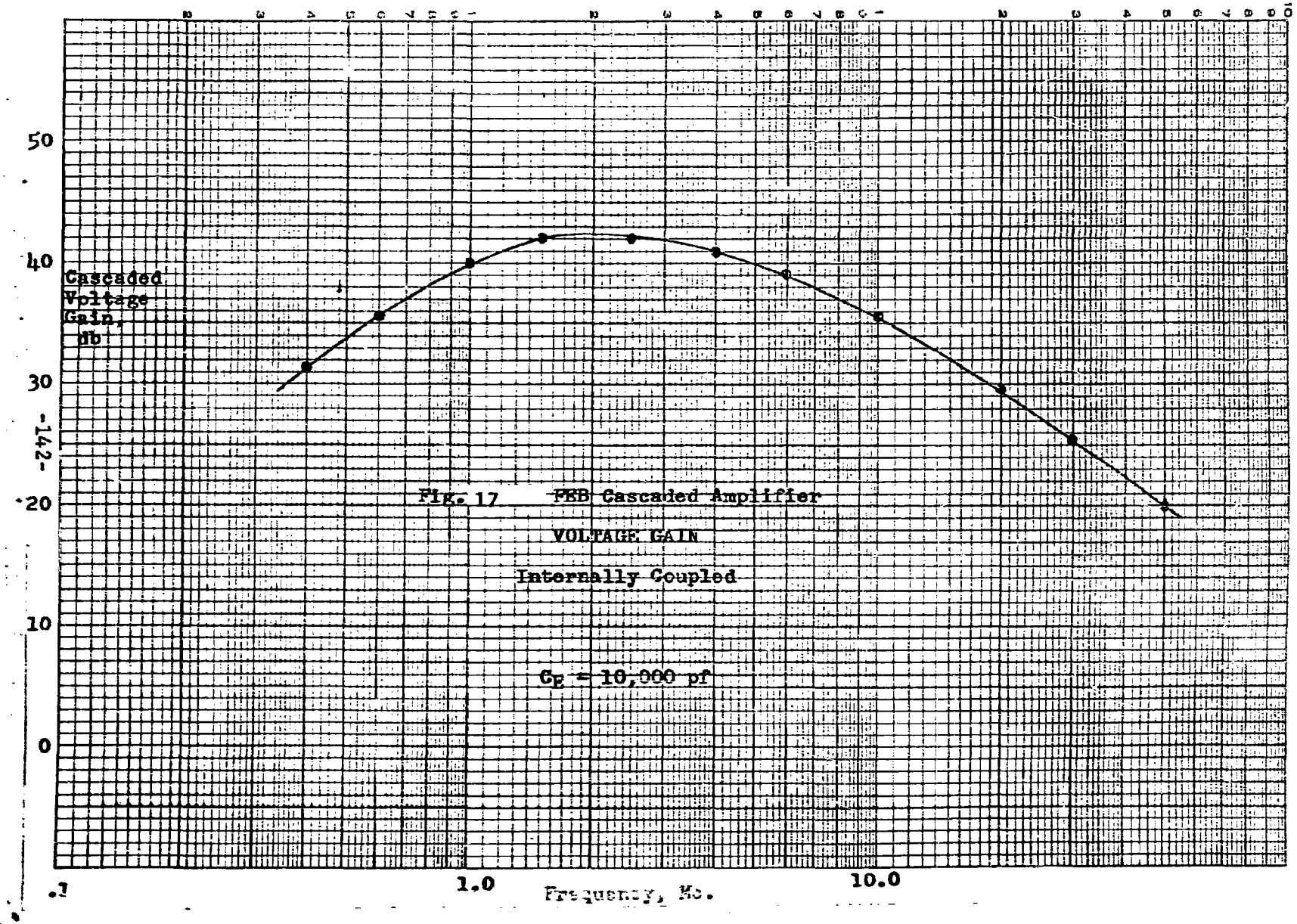


Fig. 17 PRB Cascaded Amplifier

VOLTAGE GAIN

Internally Coupled

C_E = 10,000 pf

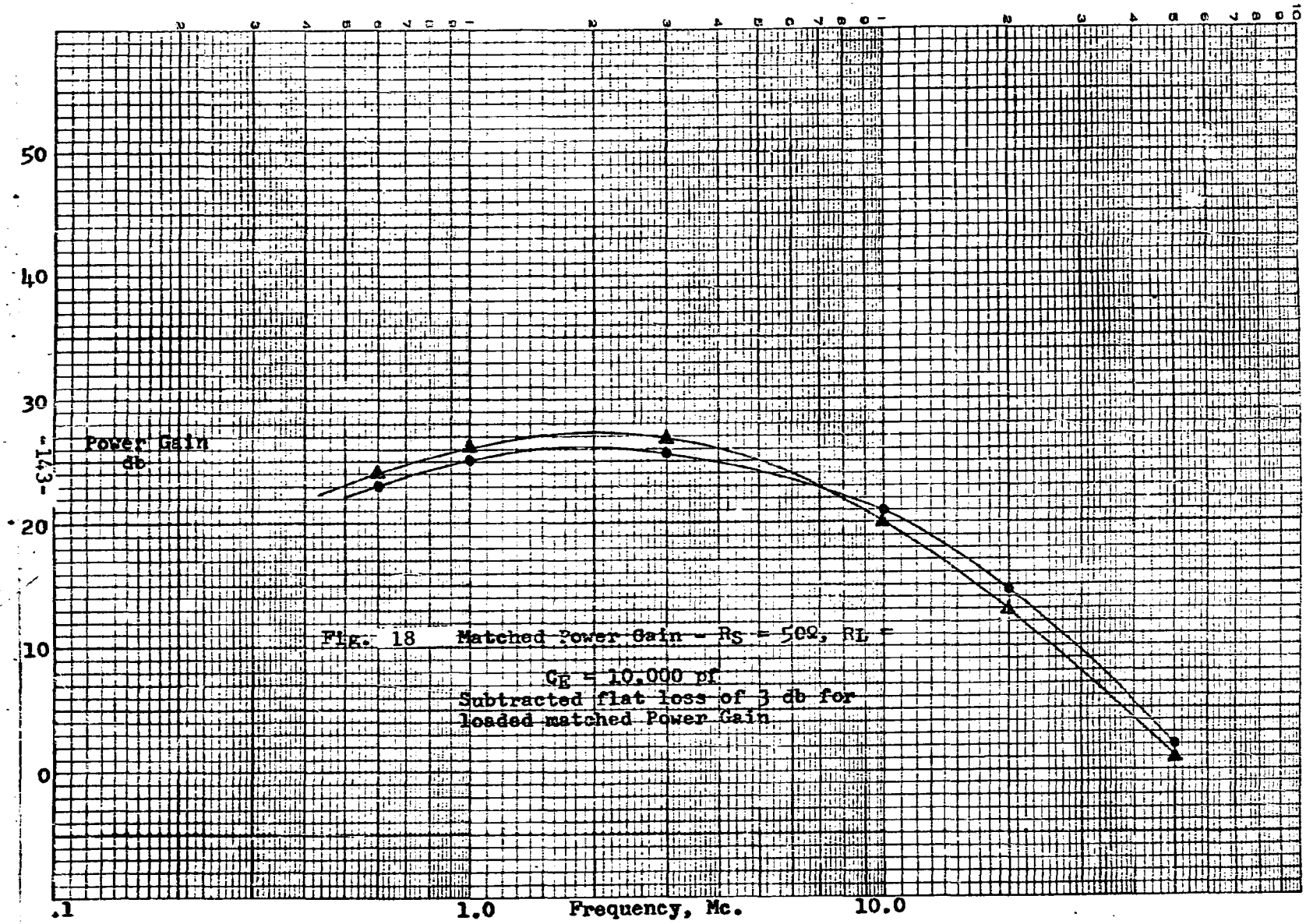


Fig. 18 Matched Power Gain - R_S = 50Ω, RL =

C_E = 10,000 pf

Subtracted flat loss of 3 db for loaded matched Power Gain

40-L310 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC-5 CYCLES X 10 DIVISIONS

EUGENE DIETZGEN CO.
PRINTED IN U. S. A.

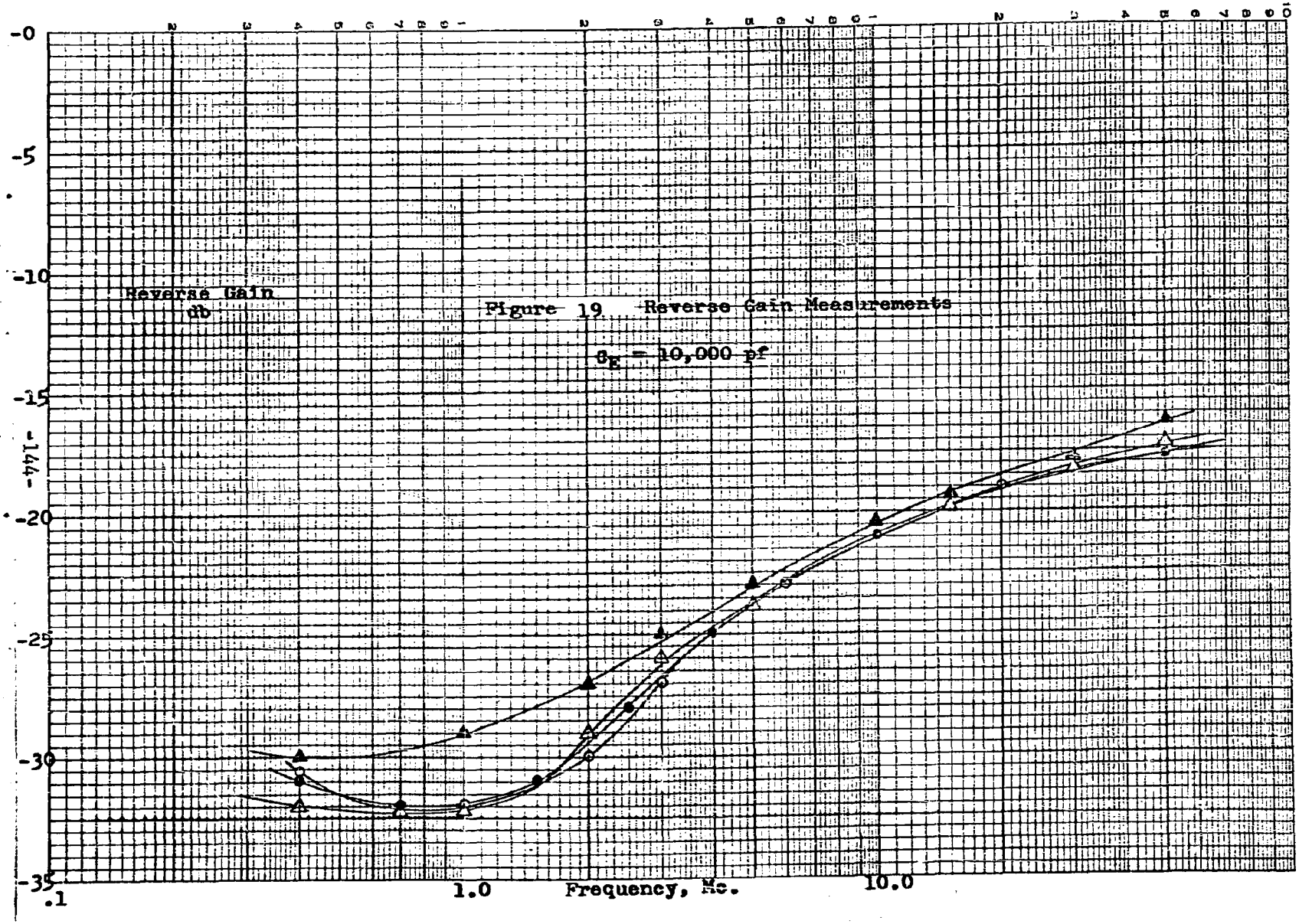


Figure 19 Reverse Gain Measurements

C_E = 10,000 pf

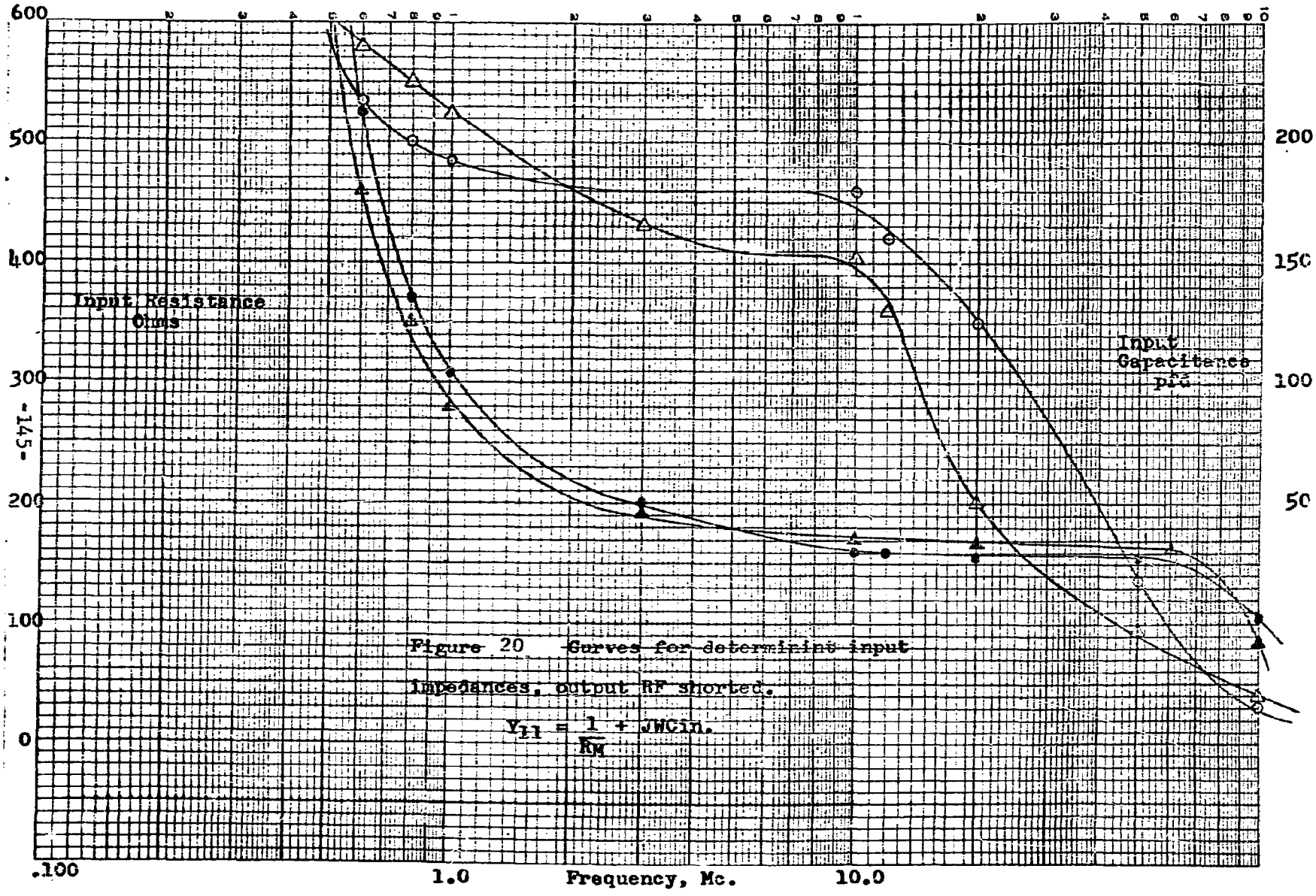


Figure 20 Curves for determining input impedances, output RF shorted.

$$Y_{11} = \frac{1}{R_{in}} + j\omega C_{in}.$$

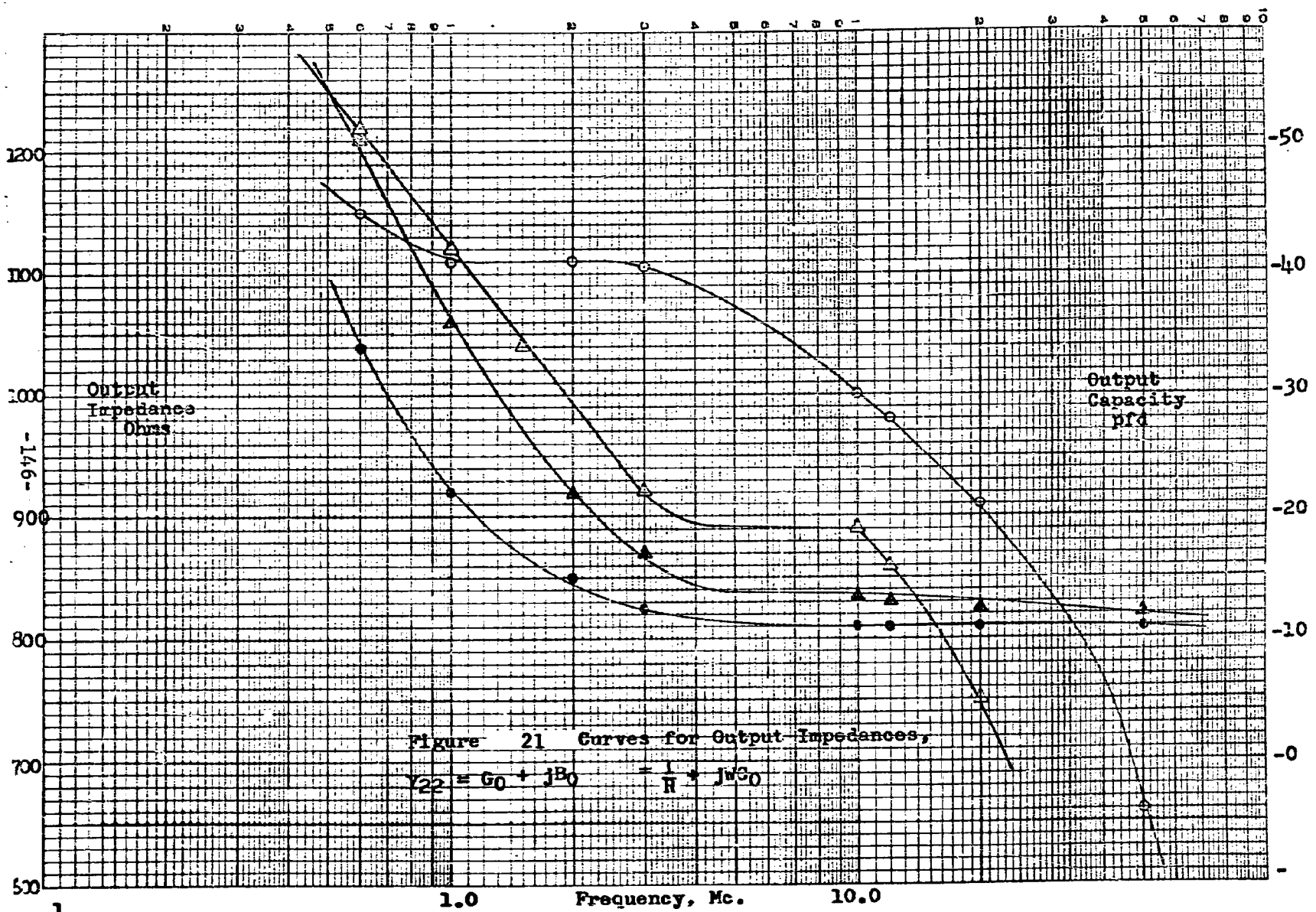


Figure 21 Curves for Output Impedances,

$Y_{22} = G_0 + jB_0 = \frac{1}{R} + j\omega C_0$

7.0 PCM TELEMETRY SYSTEM

7.1 Multiplexer Switching

The field-effect transistor was selected as the multiplexer switch. The major problems involved are transient performance and switch-drive circuitry. The major advantages to be realized are low-off-set voltage, low leakage, no transistor matching or selection, and ready application to integrated circuit implementation.

The transients generated by switch operation have been cancelled to a high degree in this system. This cancellation is possible because the opening and closing transients are very nearly equal and of opposite polarity. Thus, by causing one switch to open when another closes, their effects are minimized by near cancellation.

Several circuits have been investigated for the drive of the FET as a switch. Two of these have proven adequate for switch performance. The two drive circuits are amenable to integrated circuit implementation because all transformers have been eliminated and other components are reasonable values. See Figure 1.

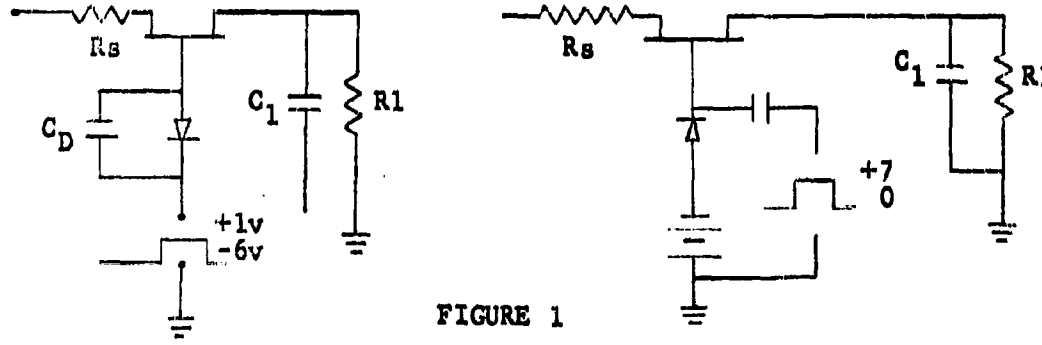


FIGURE 1

7.2 Comparator Amplifier

A preliminary comparator design has been completed. The primary problem has been one of obtaining satisfactory drift characteristics without using potentiometers or high precision resistors. An alternate approach to eliminating draft effects is one of using A.C. chopping techniques. This approach requires a considerable increase in hardware, and has been temporarily set aside as being undesirable. An operational philosophy which permits the direct transmission of the drift rather than eliminating it is also being considered as a possibility for a practical integrated circuits system.

Two basic problems are encountered when considering drift. One is the initial offset caused by circuit parameter unbalance, and the other is change in offset caused by variations in circuit parameters as a function of time, temperature, etc. The nominal offset can be adjusted to a minimum with a variable circuit element such as a potentiometer. For integrated circuits, potentiometers are not feasible and a feedback method of minimizing offset is being investigated. The variations in offset due to temperature, time, etc. appear to be reasonable in a test which has been performed. The test showed that the change in offset voltage over a 25°C temperature range was less than 2 millivolts.

A breadboard of the comparator amplifier was constructed and tested. The gain of the amplifier is 3,100 with an essentially flat response to 100KC. Adding the parasitics, which it is expected that the integrated circuits version will have, caused only a slight degradation of the frequency response.

A design modification of this circuit is needed to reduce some resistance values for ease of integration and to guarantee operation under the worst cases as imposed by the possible variations of the integrated circuits parameters.

7.3 Isolation Amplifier

A high input impedance amplifier is needed for isolation purposes. The design goals of this amplifier are:

Input Impedance	10 Megohm
Output Impedance	100 Ohm Max.
Gain	1
Gain Stability	.02%
Linearity	.04%
Off-set Voltage and Drift	Not specified as AG coupling will be used

7.4 Encoder/Decoder

The logical design of the encoder, which generates a 64 bit Reed-Muller coded word from the seven data bits, has been completed.

Work is continuing on determining the most efficient method of decoding the 64 bit Reed-Muller word into a seven bit data word using majority decision logic.

An investigation is being made into the use of a second order Reed-Muller coded word to generate the frame sync.

UNCLASSIFIED